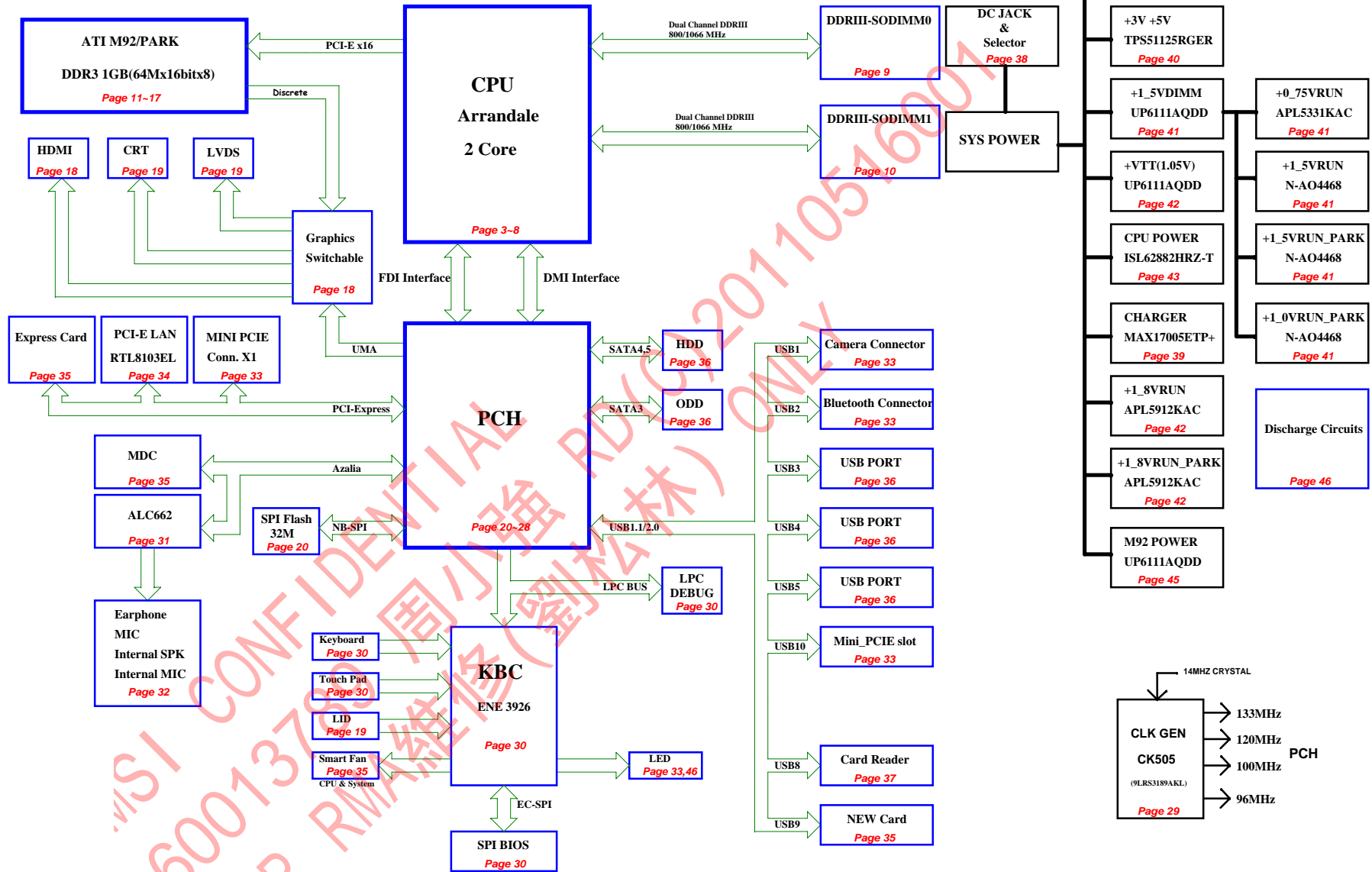


# MS-1453(Switchable) & MS-1454(UMA) Ver : 12

2010/02/01

## Calpella Platform

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05	PROCESSOR-3 (POWER)
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07	PROCESSOR-5 (GND)
08	PROCESSOR-6 (RESERVE)
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10	DDR3 SODIMM 1
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13	M92/Park-Sx(MEM_Interface)
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

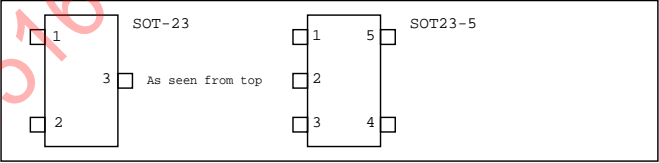
Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	LAN  DDRIII core  PCH DDRIII command & control pull up. CPU core rail Graphics core rail ( Dual Core only )
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	
+1_5VRUN	1.5V	S0,S3	
VTT	1.05V	S0	
+0_75VRUN	0.75V	S0	
+VCC_CORE	1.05V-1.1V	S0	
+VCC_GFXCORE	1.1V	S0	
M92S_VDD_CORE	0.95V	S0	
+1_8VRUN_PARK	1.8V	S0	
+1_5VRUN_PARK	1.5V	S0	
+1_0VRUN_PARK	1.0V	S0	
VDDR3	3.3V	S0	

Net Naming Conventions

Suffix
# = Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints




AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF



MICRO-STAR INT'L CO.,LTD.

Title

PLATFORM

Size

Document Number

Rev

Custom

MS-145X

12

Date:

Thursday, February 11, 2010

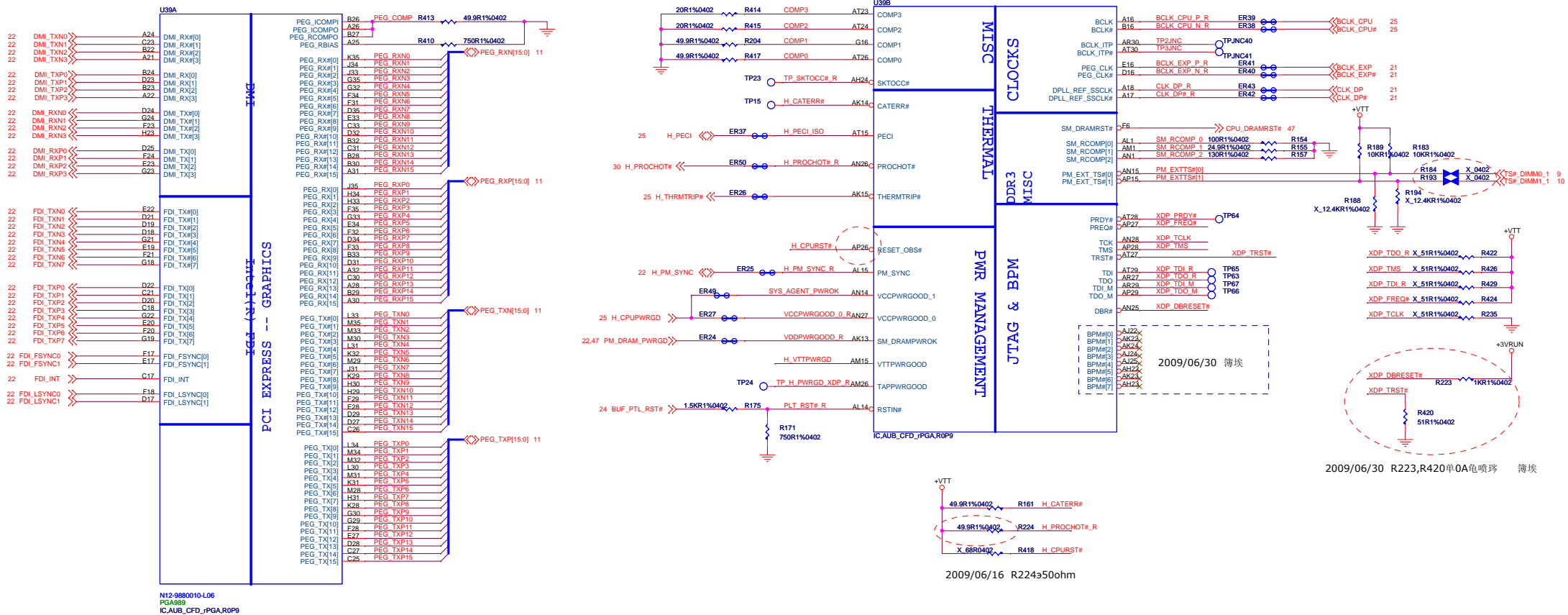
Sheet

2

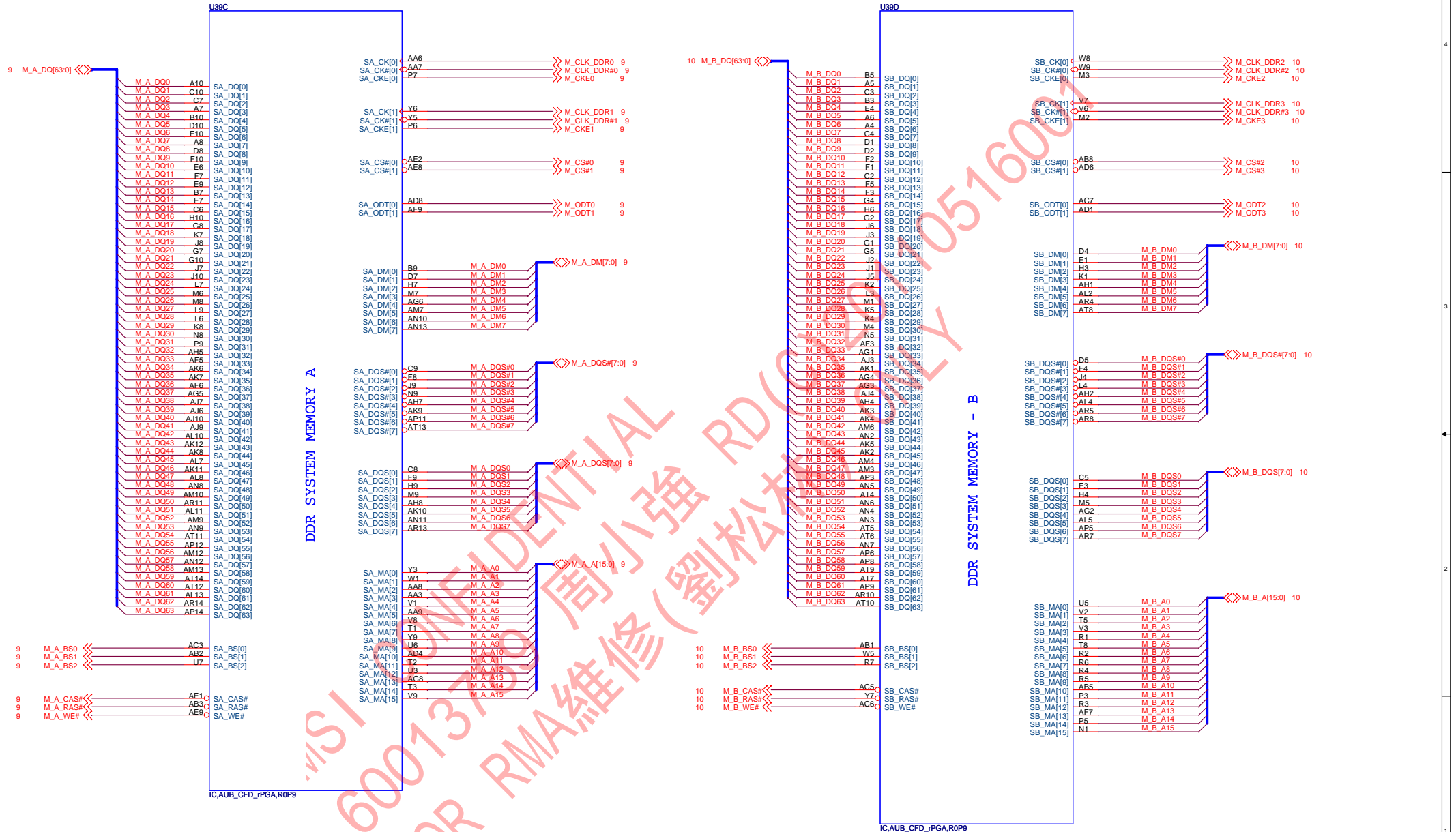
of

56

## ARRANDALE PROCESSOR (CLK,MISC,JTAG)



# ARRANDALE PROCESSOR (DDR3)

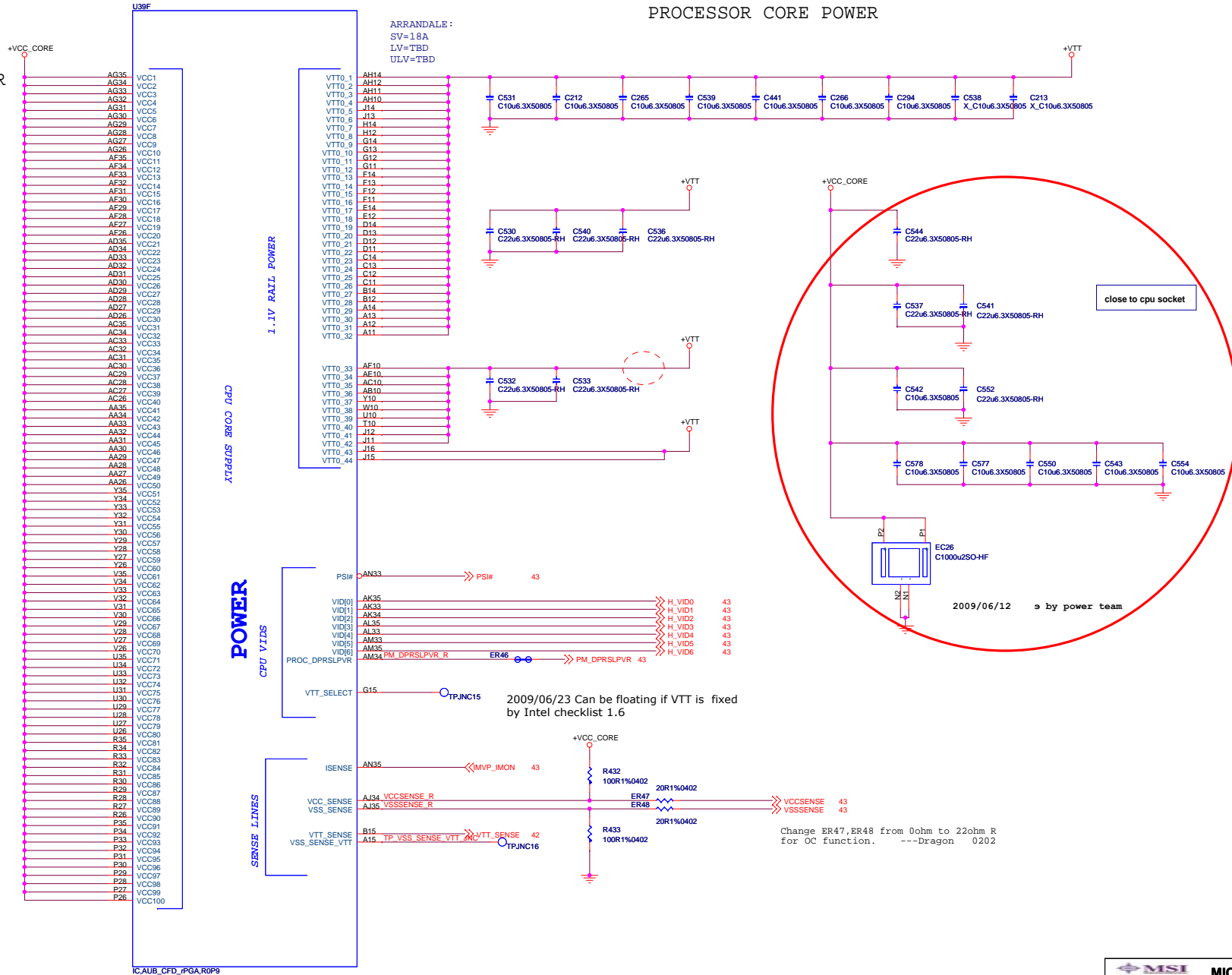


# ARRANDALE PROCESSOR (POWER)

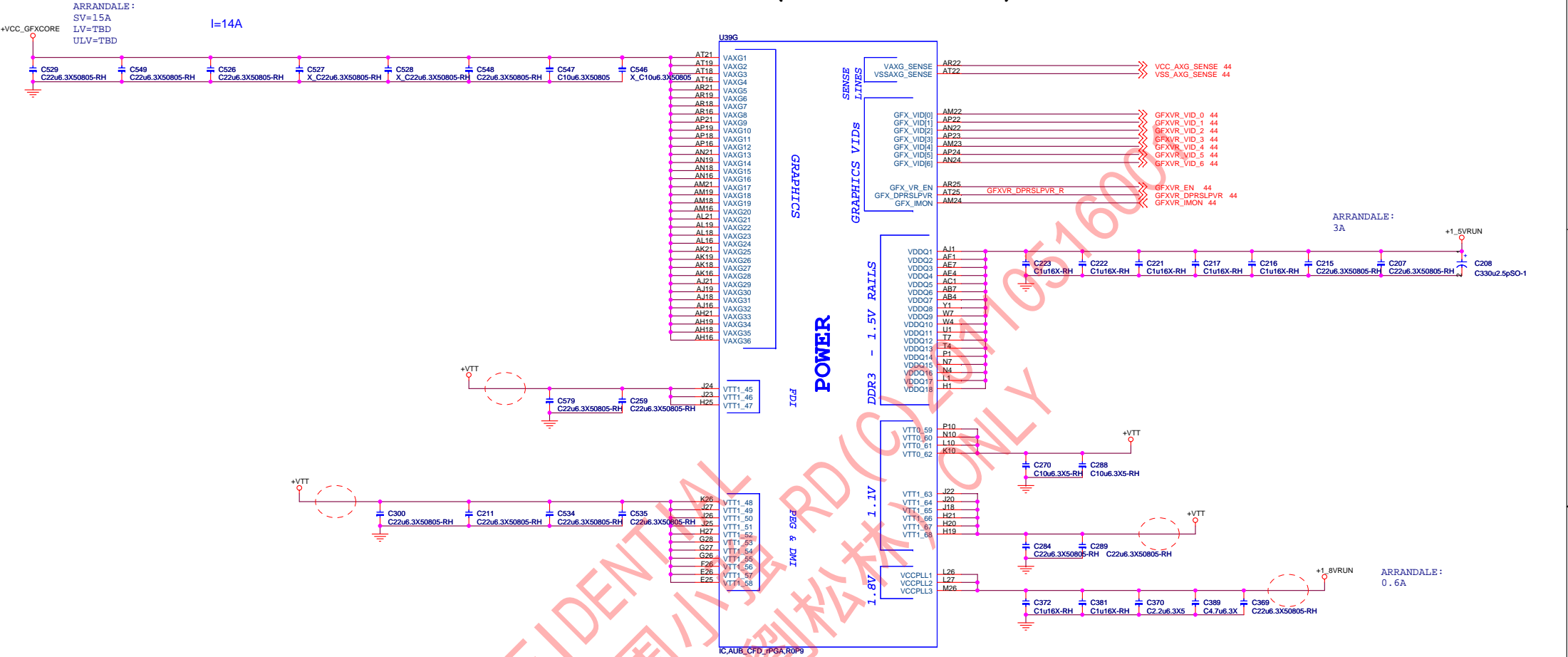
ARRANDALE:  
SV=48A  
LV=35A  
ULV=27A

## PROCESSOR CORE POWER

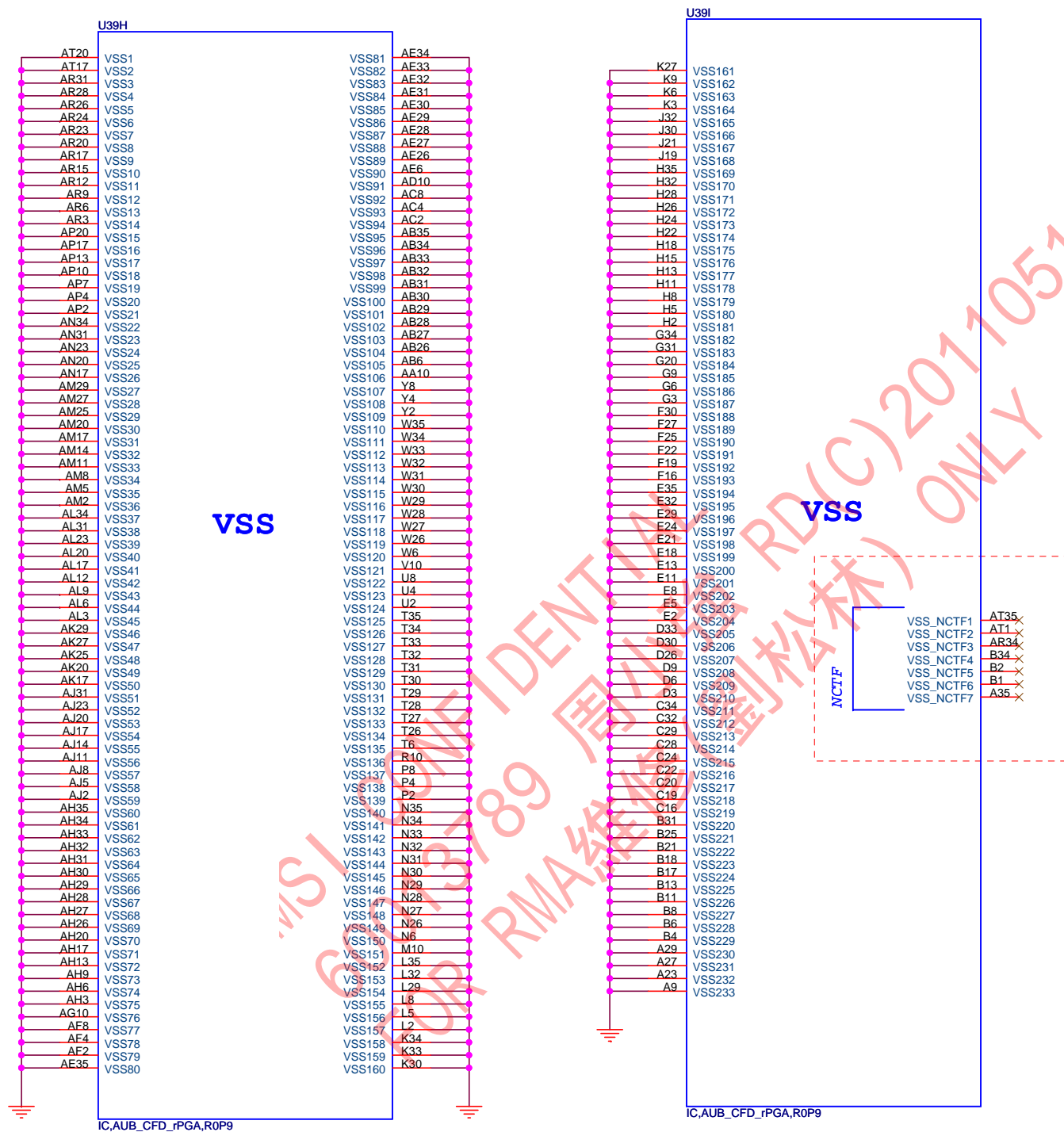
## PROCESSOR CORE POWER




ARRANDALE PROCESSOR (GRAPHICS POWER)



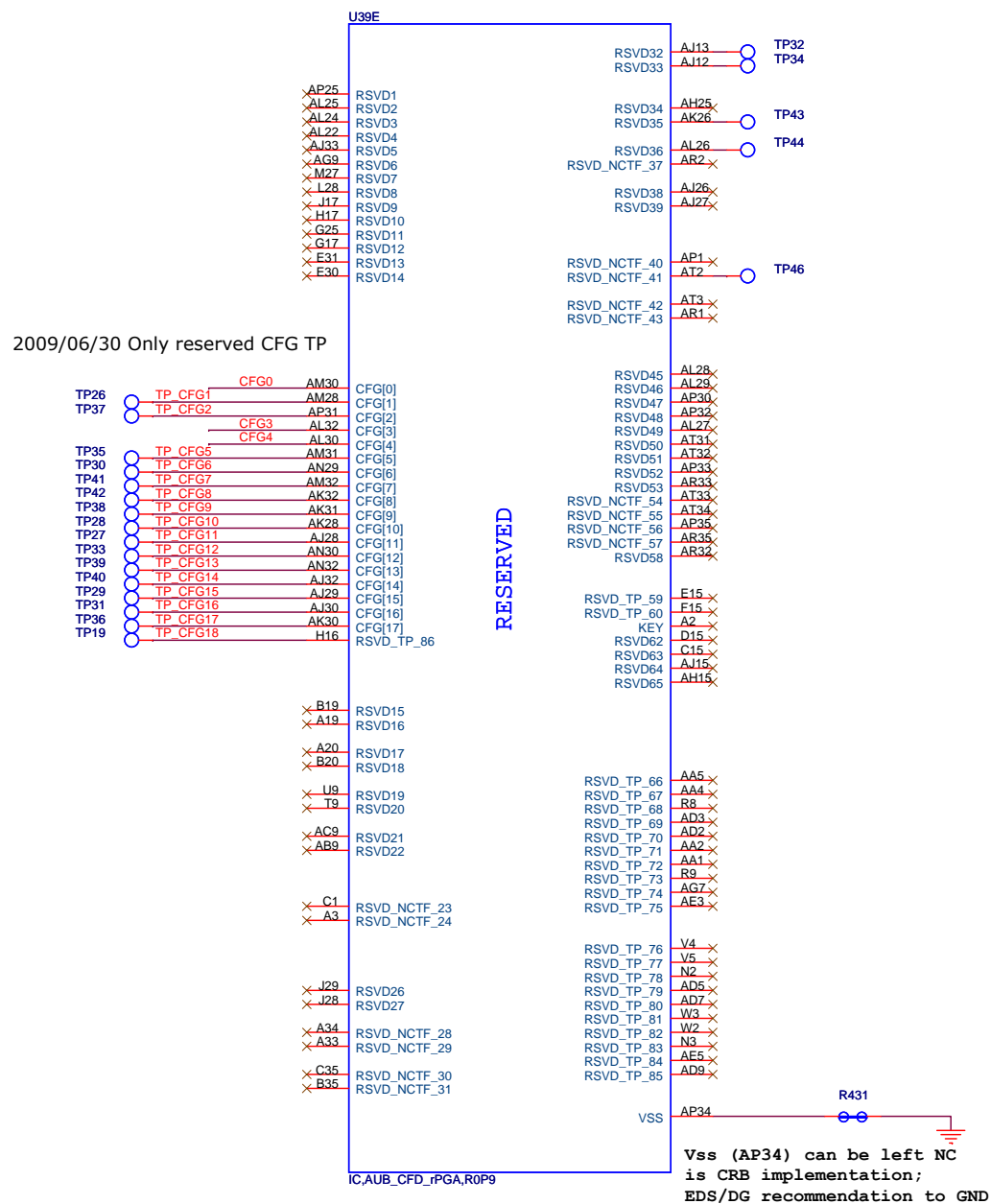
## ARRANDALE PROCESSOR (GND)



 <b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>PROCESSOR GND</b>	
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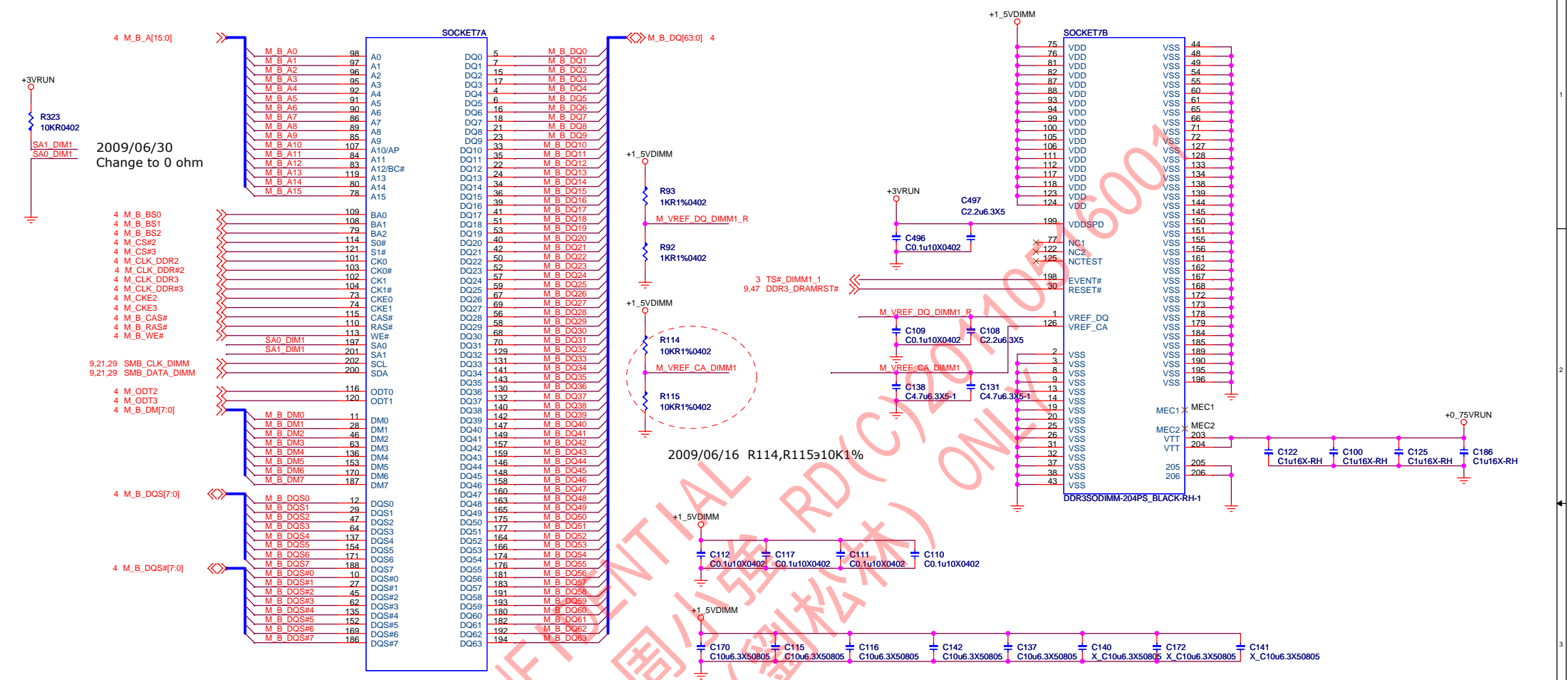
# ARRANDALE PROCESSOR (RESERVED)







SODIMM#B



2009/06/30 緯 CPU(TX)

PEG_TXP0	C555	C0.1u10X0402	GFX_RXP0	AF30	PCIE_RX0P
PEG_TXN0	C557	C0.1u10X0402	GFX_RXN0	AE31	PCIE_RX0N
PEG_TXP1	C559	C0.1u10X0402	GFX_RXP1	AE29	PCIE_RX1P
PEG_TXN1	C561	C0.1u10X0402	GFX_RXN1	AD28	PCIE_RX1N
PEG_TXP2	C563	C0.1u10X0402	GFX_RXP2	AD30	PCIE_RX2P
PEG_TXN2	C564	C0.1u10X0402	GFX_RXN2	AC31	PCIE_RX2N
PEG_TXP3	C565	C0.1u10X0402	GFX_RXP3	AC29	PCIE_RX3P
PEG_TXN3	C566	C0.1u10X0402	GFX_RXN3	AB28	PCIE_RX3N
PEG_TXP4	C567	C0.1u10X0402	GFX_RXP4	AB30	PCIE_RX4P
PEG_TXN4	C570	C0.1u10X0402	GFX_RXN4	AA31	PCIE_RX4N
PEG_TXP5	C572	C0.1u10X0402	GFX_RXP5	AA29	PCIE_RX5P
PEG_TXN5	C573	C0.1u10X0402	GFX_RXN5	Y28	PCIE_RX5N
PEG_TXP6	C574	C0.1u10X0402	GFX_RXP6	Y30	PCIE_RX6P
PEG_TXN6	C575	C0.1u10X0402	GFX_RXN6	W31	PCIE_RX6N
PEG_TXP7	C576	C0.1u10X0402	GFX_RXP7	W29	PCIE_RX7P
PEG_TXN7	C586	C0.1u10X0402	GFX_RXN7	V28	PCIE_RX7N
PEG_TXP8	C587	C0.1u10X0402	GFX_RXP8	V30	PCIE_RX8P
PEG_TXN8	C588	C0.1u10X0402	GFX_RXN8	U31	PCIE_RX8N
PEG_TXP9	C596	C0.1u10X0402	GFX_RXP9	U29	PCIE_RX9P
PEG_TXN9	C595	C0.1u10X0402	GFX_RXN9	T28	PCIE_RX9N
PEG_TXP10	C585	C0.1u10X0402	GFX_RXP10	T30	PCIE_RX10P
PEG_TXN10	C584	C0.1u10X0402	GFX_RXN10	R31	PCIE_RX10N
PEG_TXP11	C594	C0.1u10X0402	GFX_RXP11	R29	PCIE_RX11P
PEG_TXN11	C593	C0.1u10X0402	GFX_RXN11	P28	PCIE_RX11N
PEG_TXP12	C583	C0.1u10X0402	GFX_RXP12	P30	PCIE_RX12P
PEG_TXN12	C582	C0.1u10X0402	GFX_RXN12	N31	PCIE_RX12N
PEG_TXP13	C592	C0.1u10X0402	GFX_RXP13	N29	PCIE_RX13P
PEG_TXN13	C591	C0.1u10X0402	GFX_RXN13	M28	PCIE_RX13N
PEG_TXP14	C581	C0.1u10X0402	GFX_RXP14	M30	PCIE_RX14P
PEG_TXN14	C580	C0.1u10X0402	GFX_RXN14	L31	PCIE_RX14N
PEG_TXP15	C590	C0.1u10X0402	GFX_RXP15	L29	PCIE_RX15P
PEG_TXN15	C589	C0.1u10X0402	GFX_RXN15	K30	PCIE_RX15N

U40A

PCI EXPRESS INTERFACE

PCIE_TX0P	AH30	GFX_TXP0	C260	C0.1u10X0402	PEG_RXP0
PCIE_TX0N	AG31	GFX_TXN0	C264	C0.1u10X0402	PEG_RXN0
PCIE_TX1P	AG29	GFX_TXP1	C267	C0.1u10X0402	PEG_RXP1
PCIE_TX1N	AF28	GFX_TXN1	C263	C0.1u10X0402	PEG_RXN1
PCIE_TX2P	AF27	GFX_TXP2	C272	C0.1u10X0402	PEG_RXP2
PCIE_TX2N	AF26	GFX_TXN2	C268	C0.1u10X0402	PEG_RXN2
PCIE_TX3P	AD27	GFX_TXP3	C271	C0.1u10X0402	PEG_RXP3
PCIE_TX3N	AD26	GFX_TXN3	C276	C0.1u10X0402	PEG_RXN3
PCIE_TX4P	AC25	GFX_TXP4	C287	C0.1u10X0402	PEG_RXP4
PCIE_TX4N	AB25	GFX_TXN4	C283	C0.1u10X0402	PEG_RXN4
PCIE_TX5P	Y23	GFX_TXP5	C286	C0.1u10X0402	PEG_RXP5
PCIE_TX5N	Y24	GFX_TXN5	C291	C0.1u10X0402	PEG_RXN5
PCIE_TX6P	AB27	GFX_TXP6	C295	C0.1u10X0402	PEG_RXP6
PCIE_TX6N	AB26	GFX_TXN6	C299	C0.1u10X0402	PEG_RXN6
PCIE_TX7P	Y27	GFX_TXP7	C298	C0.1u10X0402	PEG_RXP7
PCIE_TX7N	Y26	GFX_TXN7	C302	C0.1u10X0402	PEG_RXN7
PCIE_TX8P	W24	GFX_TXP8	C304	C0.1u10X0402	PEG_RXP8
PCIE_TX8N	W23	GFX_TXN8	C313	C0.1u10X0402	PEG_RXN8
PCIE_TX9P	Y27	GFX_TXP9	C307	C0.1u10X0402	PEG_RXP9
PCIE_TX9N	U26	GFX_TXN9	C314	C0.1u10X0402	PEG_RXN9
PCIE_TX10P	U24	GFX_TXP10	C318	C0.1u10X0402	PEG_RXP10
PCIE_TX10N	U23	GFX_TXN10	C323	C0.1u10X0402	PEG_RXN10
PCIE_TX11P	T26	GFX_TXP11	C322	C0.1u10X0402	PEG_RXP11
PCIE_TX11N	T27	GFX_TXN11	C325	C0.1u10X0402	PEG_RXN11
PCIE_TX12P	T24	GFX_TXP12	C329	C0.1u10X0402	PEG_RXP12
PCIE_TX12N	T23	GFX_TXN12	C333	C0.1u10X0402	PEG_RXN12
PCIE_TX13P	P27	GFX_TXP13	C332	C0.1u10X0402	PEG_RXP13
PCIE_TX13N	P26	GFX_TXN13	C336	C0.1u10X0402	PEG_RXN13
PCIE_TX14P	P24	GFX_TXP14	C343	C0.1u10X0402	PEG_RXP14
PCIE_TX14N	P23	GFX_TXN14	C347	C0.1u10X0402	PEG_RXN14
PCIE_TX15P	M27	GFX_TXP15	C348	C0.1u10X0402	PEG_RXP15
PCIE_TX15N	N26	GFX_TXN15	C345	C0.1u10X0402	PEG_RXN15

PEG\_RXN[15:0] <<PEG\_RXN[15:0] 3  
PEG\_RXP[15:0] <<PEG\_RXP[15:0] 3  
PEG\_TXP[15:0] >>PEG\_TXP[15:0] 3  
PEG\_TXN[15:0] >>PEG\_TXN[15:0] 3

CLOCK

21 CLK\_PEGA\_MXM\_P >> AK30 PCIE\_REFCLKP  
21 CLK\_PEGA\_MXM\_N >> AK32 PCIE\_REFCLKN

CALIBRATION

PCIE\_CALRP Y22 VGA\_PE\_CP R203 1.27KΩ  
PCIE\_CALRN AA22 VGA\_PE\_CN R205 2KΩ 1% 0402 +1.0VRUN\_PARK

N10 PWRGOOD

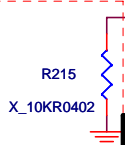
AL27 PERSTB

216-0728018-00-A2-RH


CheckResetSequence

For Park-S3: PWRGOOD pin must need to pull low


For M92-S2/S3: PWRGOOD pin should be NC



	M92-S2	PARK-S3
R215	X	-

			MICRO-STAR INT'L CO.,LTD.		
Title M92/Pak-Sx (PCIE Interface)					
Size	Document Number				Rev
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 <b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>Title</b> <b>M92/Pak-Sx (MEM Interface)</b>	
<b>Size</b> <b>Document Number</b>	<b>Rev</b>
<b>MS-145X</b>	
<b>Date:</b> <b>Thursday, February 11, 2010</b>	<b>Sheet</b> <b>13</b> <b>of</b> <b>56</b>





**1.8V@130mA**

**NOTE : 4**

**1.8V@20mA**

**LVDS Mode: 1.8V@200mA**

**(DP Mode: 1.8V@130mA)**

**1.8V@20mA**

**NOTE : 4**

[illegible]

Park-S3: 110mA@1.0V  
M9X-S2/S3: 200mA@1.1V

DPA\_VDD10

C239 X\_C10u6.3X50805  
C245 C1u6.3Y0402-RH  
C244 C0.1u10X0402-1

B13 120L600mA-250

+1\_0V/RUN\_PARK

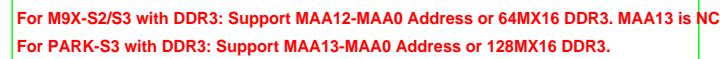
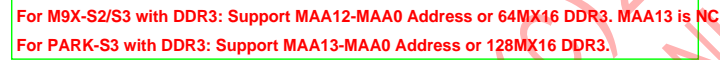
Park-S3: TMDS/DP=110mA@1.0V ; LVDS=120mA@1.0V  
M9X-S2/S3: TMDS/DP=170mA@1.1V LVDS=100mA@1.1V

DPE\_VDD10

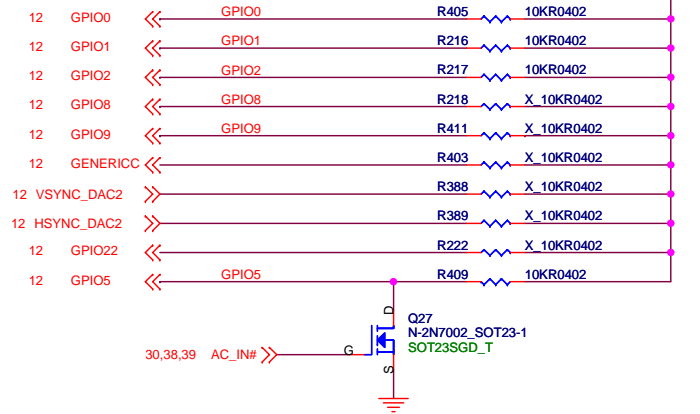
C519 X\_C10u6.3X50805  
C519 C1u6.3Y0402-RH  
C515 C0.1u10X0402-1

B20 120L600mA-250

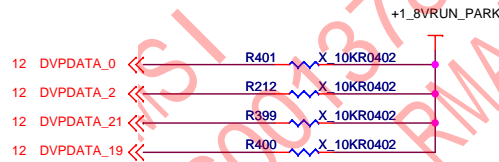
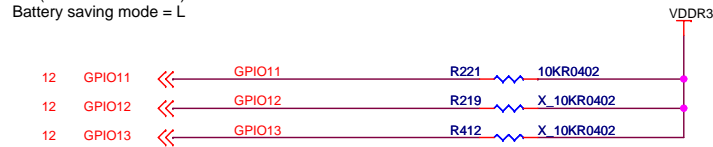




## PIN STRAPS



GPIO\_5\_AC\_BATT is an optional input which allows the system to request (AC) performance mode or battery mode operation.  
AC (Performance mode) = H  
Battery saving mode = L




## CONFIGURATION STRAPS

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
GPIO0	1		GPIO=0 50% TX output swing GPIO=1 Full TX output swing
GPIO1	1		GPIO=0 TX de-emphasis disabled GPIO=1 TX de-emphasis enabled
GPIO2	1		GPIO=0 Advertises the PCIe device as 2.5 GT/S capable at power-on GPIO=1 Advertises the PCIe device as 5 GT/S capable at power-on
GPIO9	0		GPIO=0 VGA controller capacity enabled. GPIO=1 The device will not be recognized as the system's VGA controller.
VSYNC_DAC2	0		GPIO=0 Driver would ignore the value sampled on DVPDATA_20 during reset.
GPIO22	0		GPIO=0 not used external BIOS ROM GPIO=1 if used

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
GPIO 13 GPIO 12 GPIO 11	0 0 1		0 0 0=128 MB 0 0 1=256 MB 0 1 0=64 MB

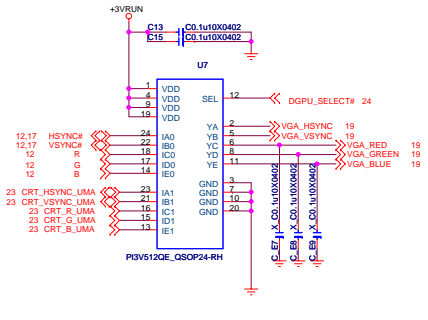
PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
VGA_HSYNC# VGA_VSYNC#	1 1		0 0=No audio function 0 1=Audio for display port only 1 0=Audio for display port and HDMI if dongle is detected 1 1=Audio for both displayport and HDMI

DVPDATA19	DVPDATA21	DVPDATA2	DVPDATA0	MEM_TYPE
0	0	0	0	Hynix 64Mx16 DDR3 (M12-5TQ1G25-H23)
0	0	0	1	Samsung 64Mx16 DDR3 (M12-K4W1G85-S02)
0	0	1	0	
0	0	1	1	

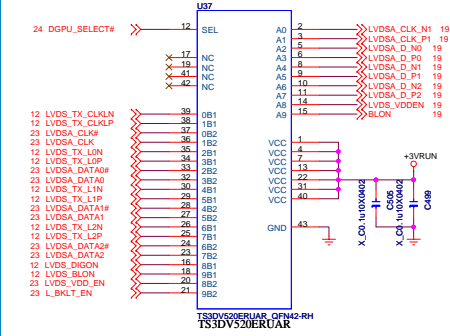
 <b>MSI</b> <i>Leading the Other Pathways</i>		<b>MICRO-STAR INT'L CO.,LTD.</b>	
Title			
<b>M92/Pak-Sx (Straps &amp; Thermal)</b>			
Size B	Document Number <b>MS-145X</b>		Rev 12
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CRT Switch

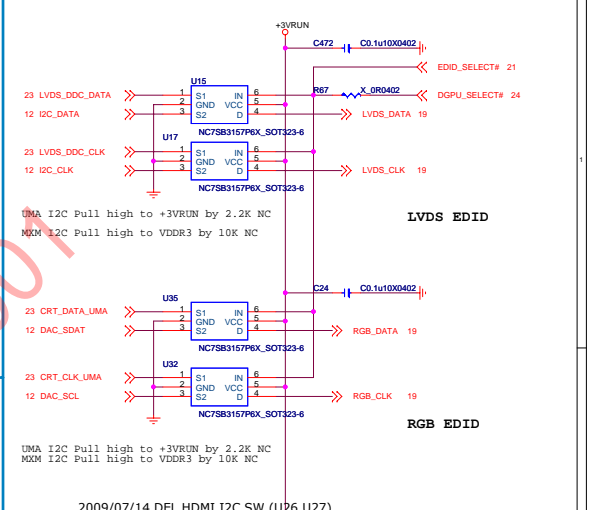
2009/07/14 Change RGB SW



LVDS Switch

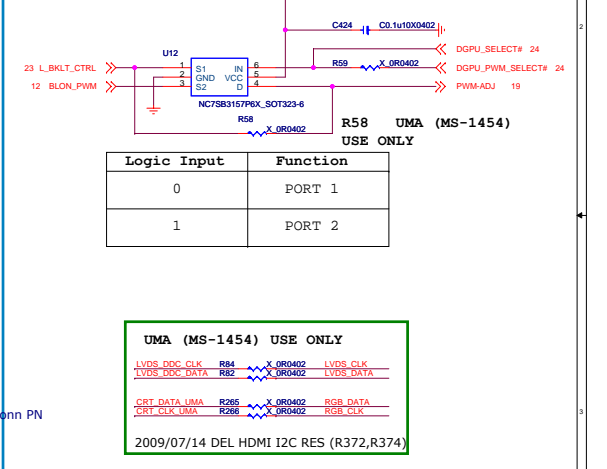
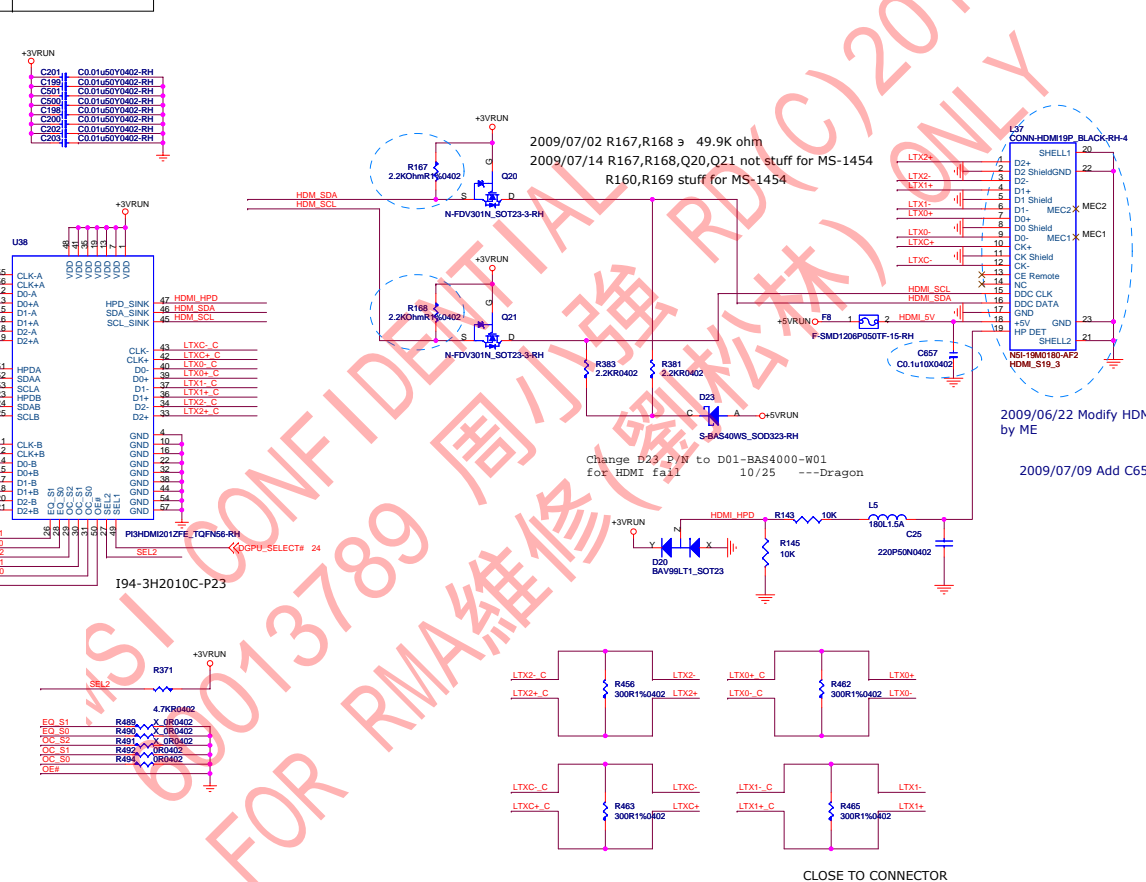
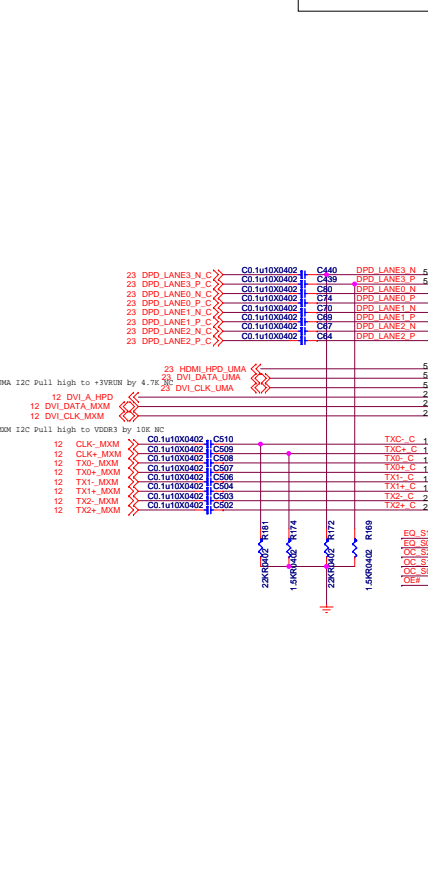


EDID Switch (CRT, LVDS)



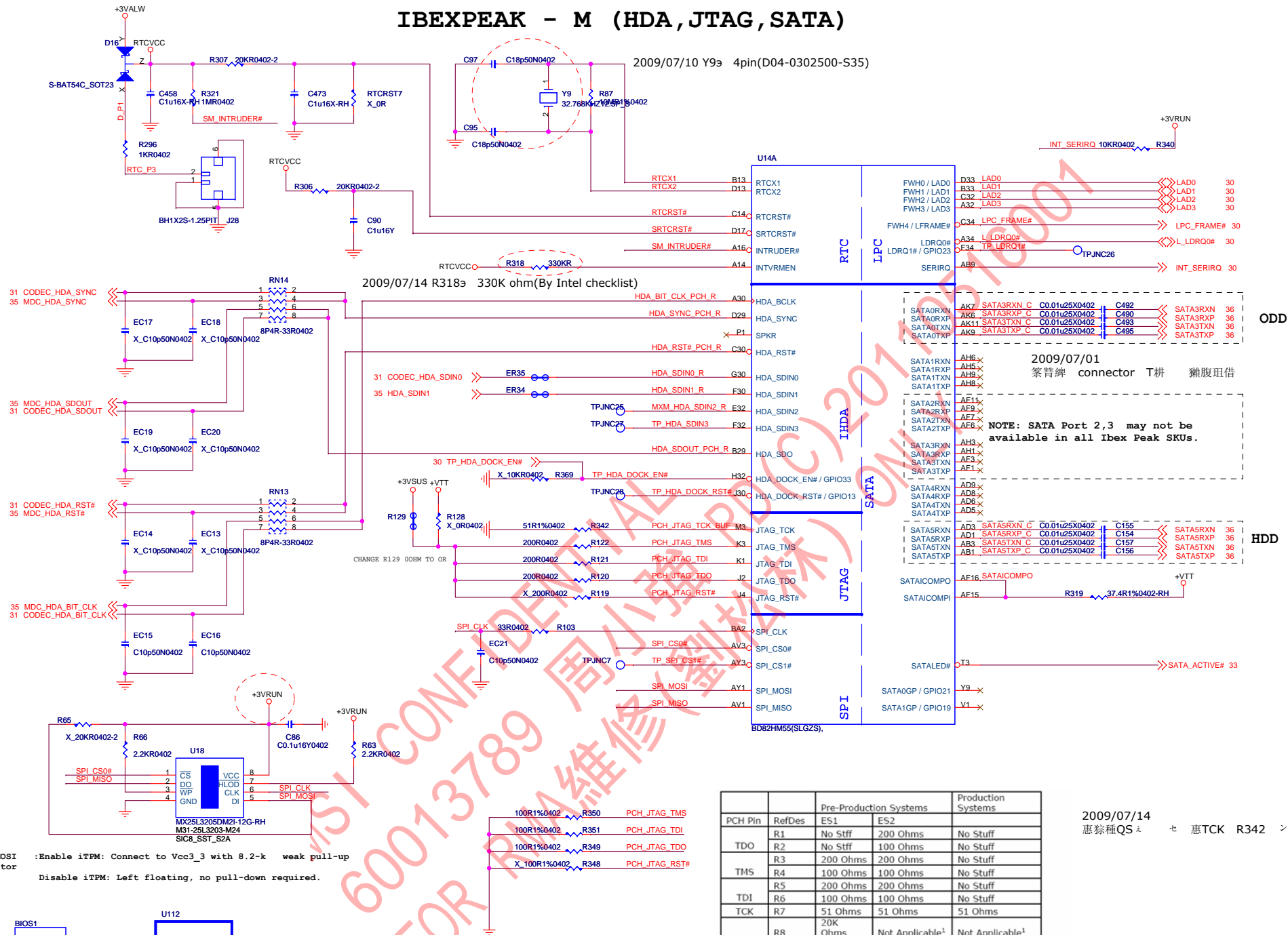
HDMI Switch

2009/07/14 Change HDMI SW





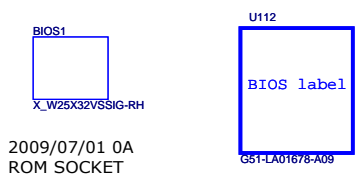
# IBEXPEAK - M (HDA, JTAG, SATA)



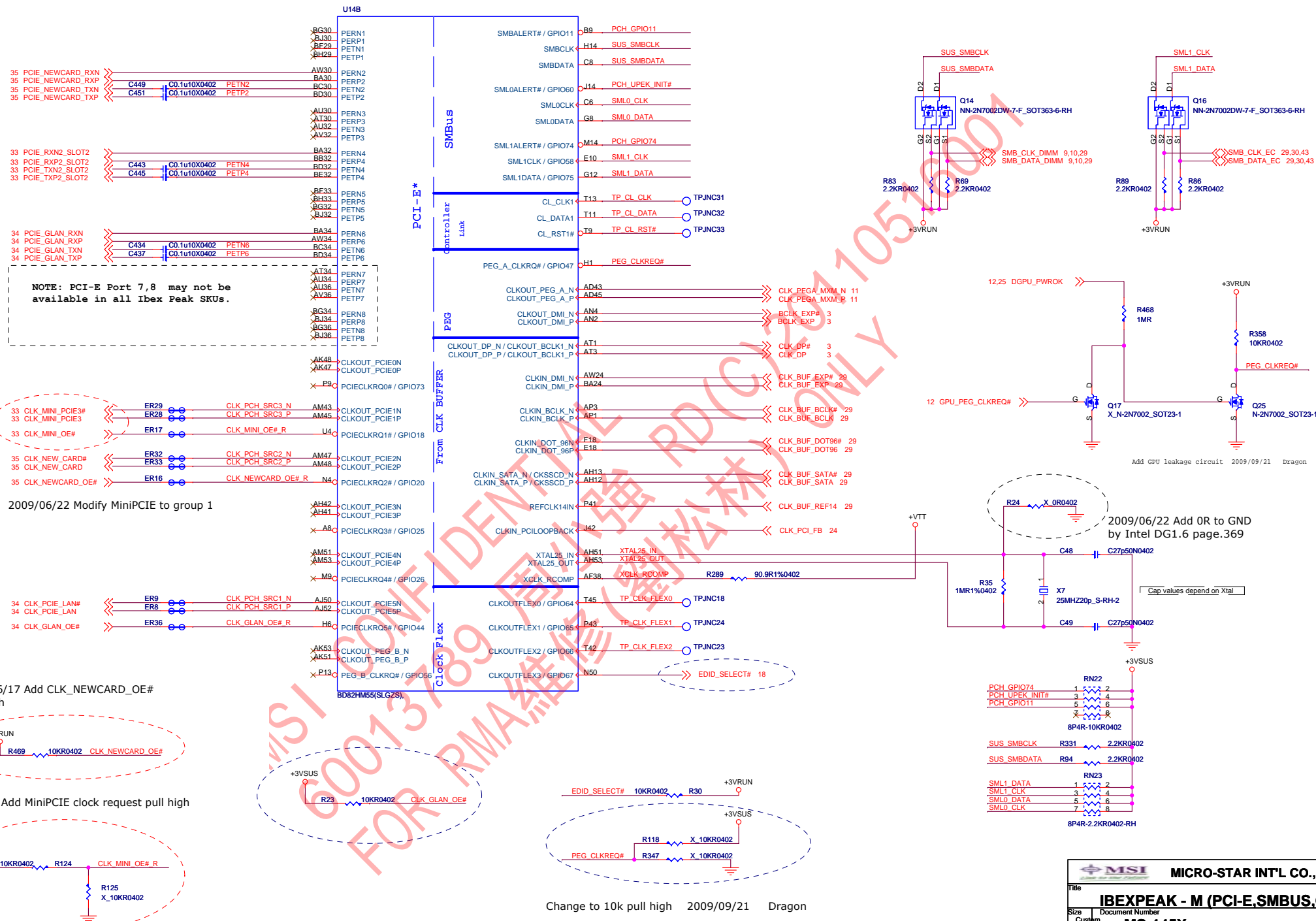
		Pre-Production Systems		Production Systems
PCH Pin	RefDes	ES1	ES2	
TDO	R1	No Stff	200 Ohms	No Stuff
	R2	No Stff	100 Ohms	No Stuff
TMS	R3	200 Ohms	200 Ohms	No Stuff
	R4	100 Ohms	100 Ohms	No Stuff
	R5	200 Ohms	200 Ohms	No Stuff
TDI	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
	R8	20K Ohms	Not Applicable <sup>1</sup>	Not Applicable <sup>1</sup>
TRST#	R9	10K Ohms	Not Applicable <sup>1</sup>	Not Applicable <sup>1</sup>

Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes

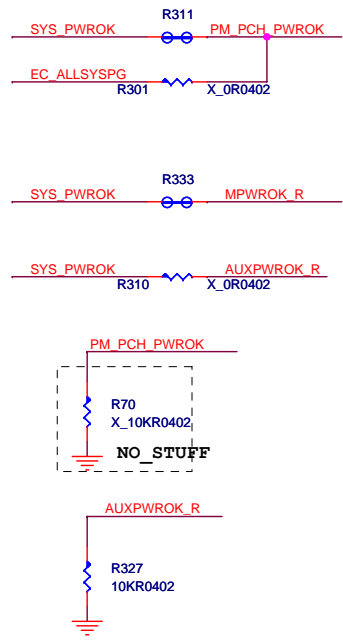
<b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>IBEXPEAK - M (HDA,JTAG,SATA)</b>	
Size	Document Number
Custom	<b>MS-145X</b>
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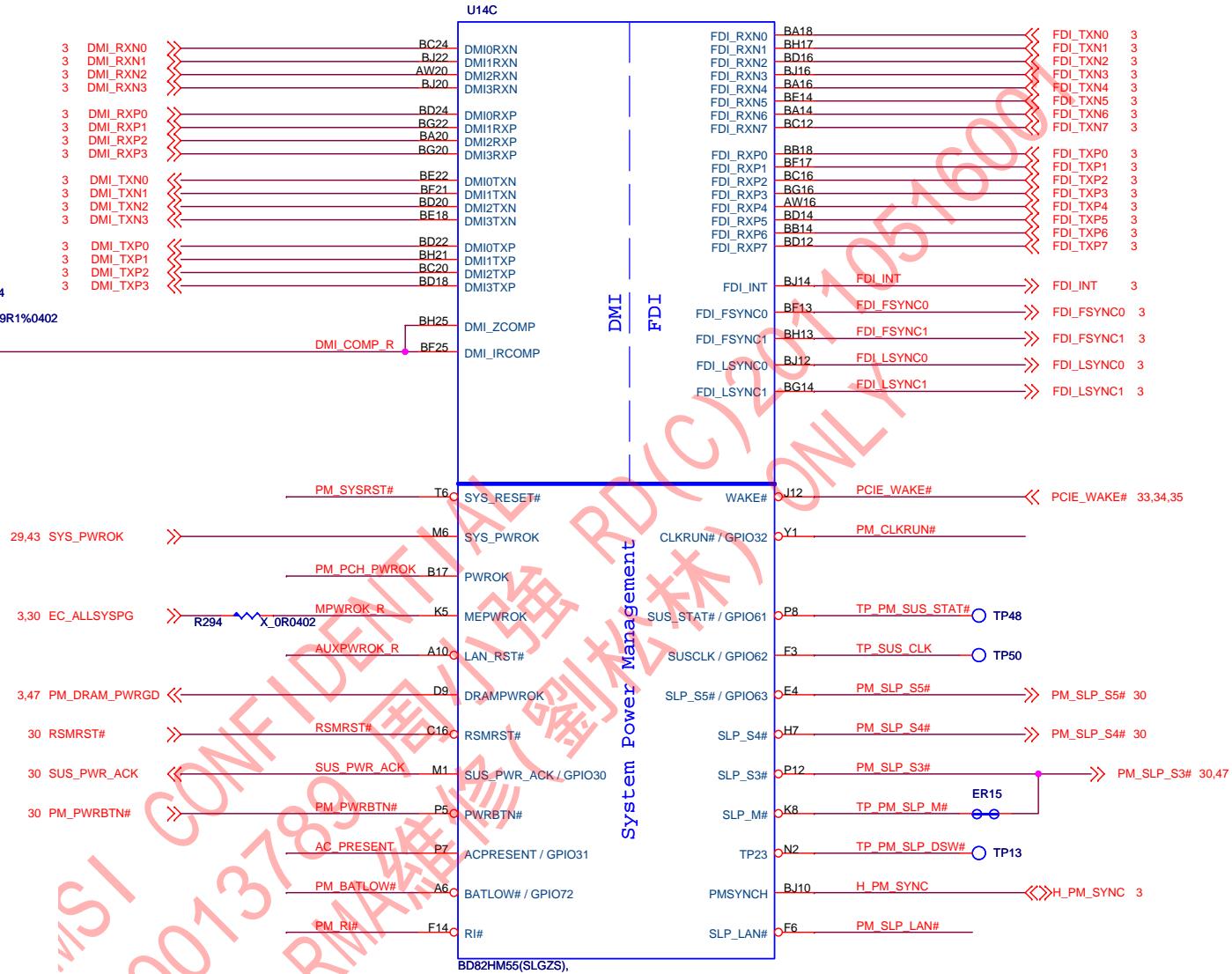
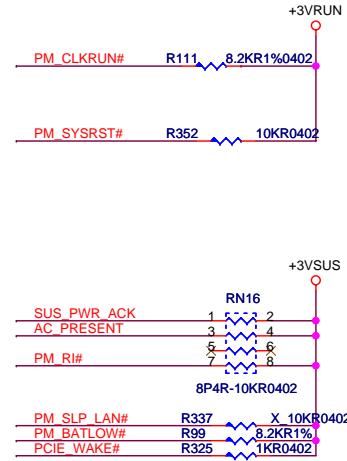
**IBEXPEAK - M (PCI-E, SMBUS, CLK)**



# IBEXPEAK - M (DMI, FDI, GPIO)



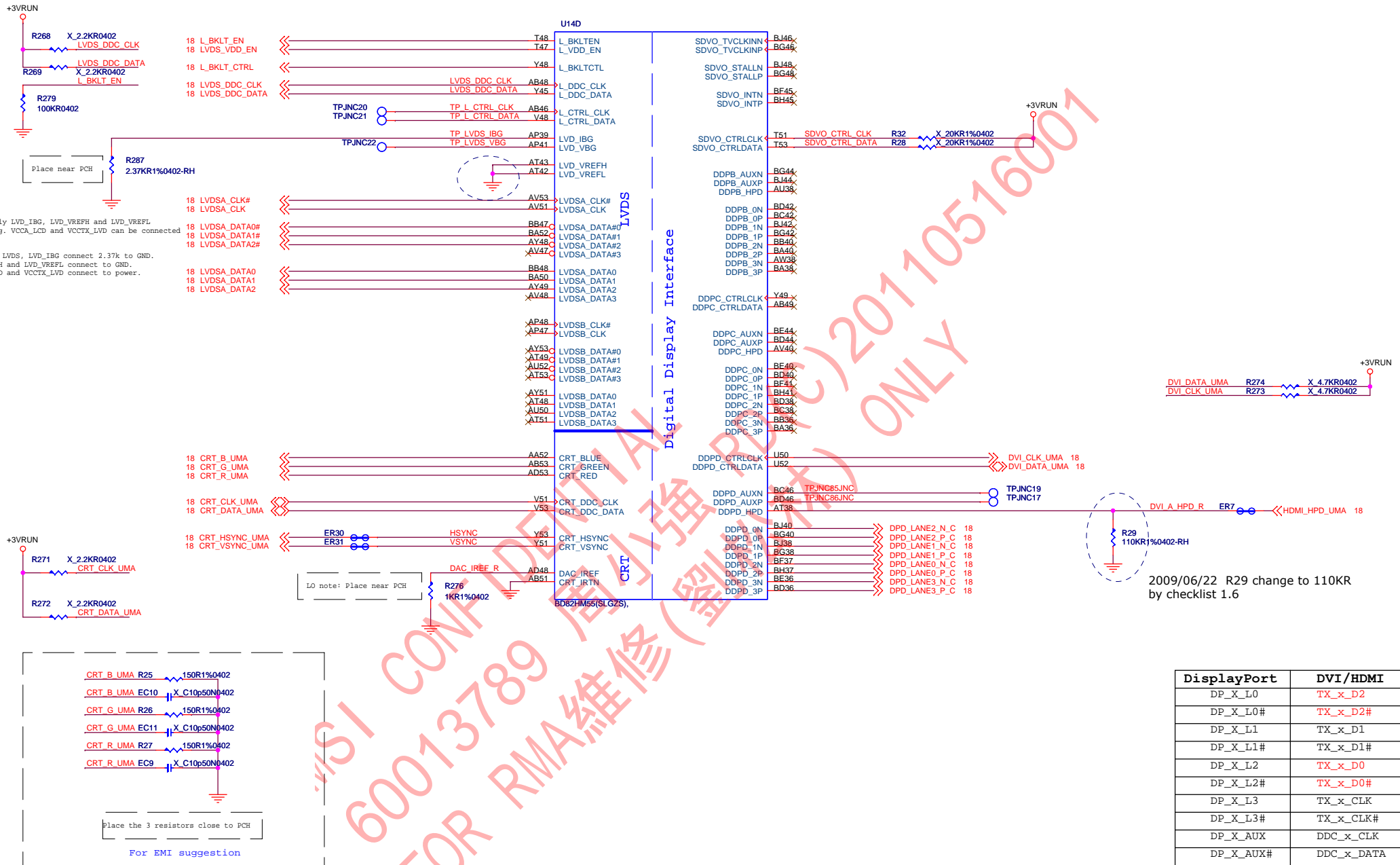
PULL LOW FOR NOT INTEL LAN 2008.12.12



		MICRO-STAR INT'L CO.,LTD.	
Title			
IBEXPEAK - M (DMI,FDI,GPIO)			
Size	Document Number		Rev
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# IBEXPEAK - M (LVDS,DDI)



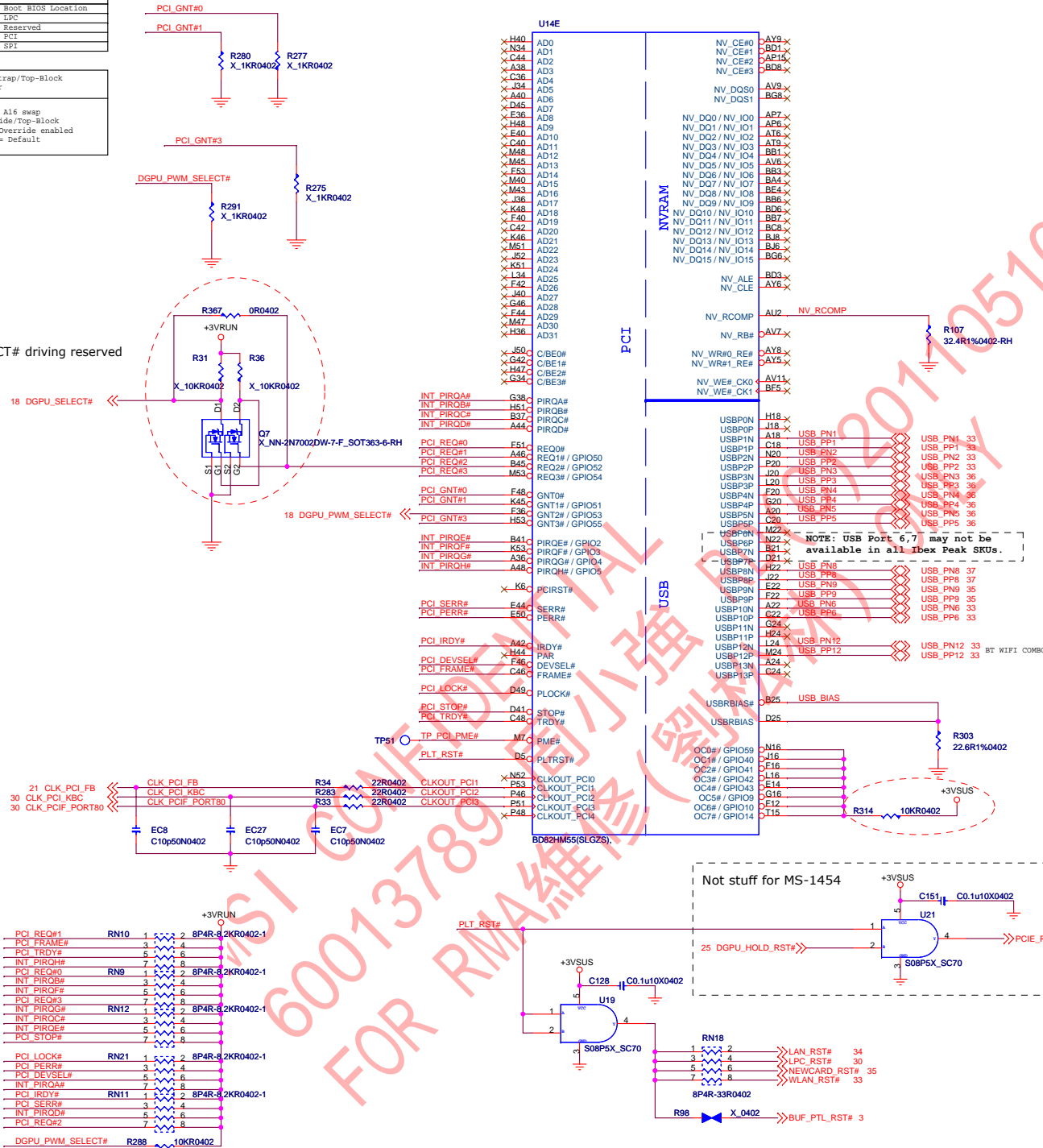
DisplayPort	DVI/HDMI
DP_X_I0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

# IBEXPEAK - M (PCI,USB,NVRAM)

PCI_GNT#0	PCI_GNT#1	Boot BIOS location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPi

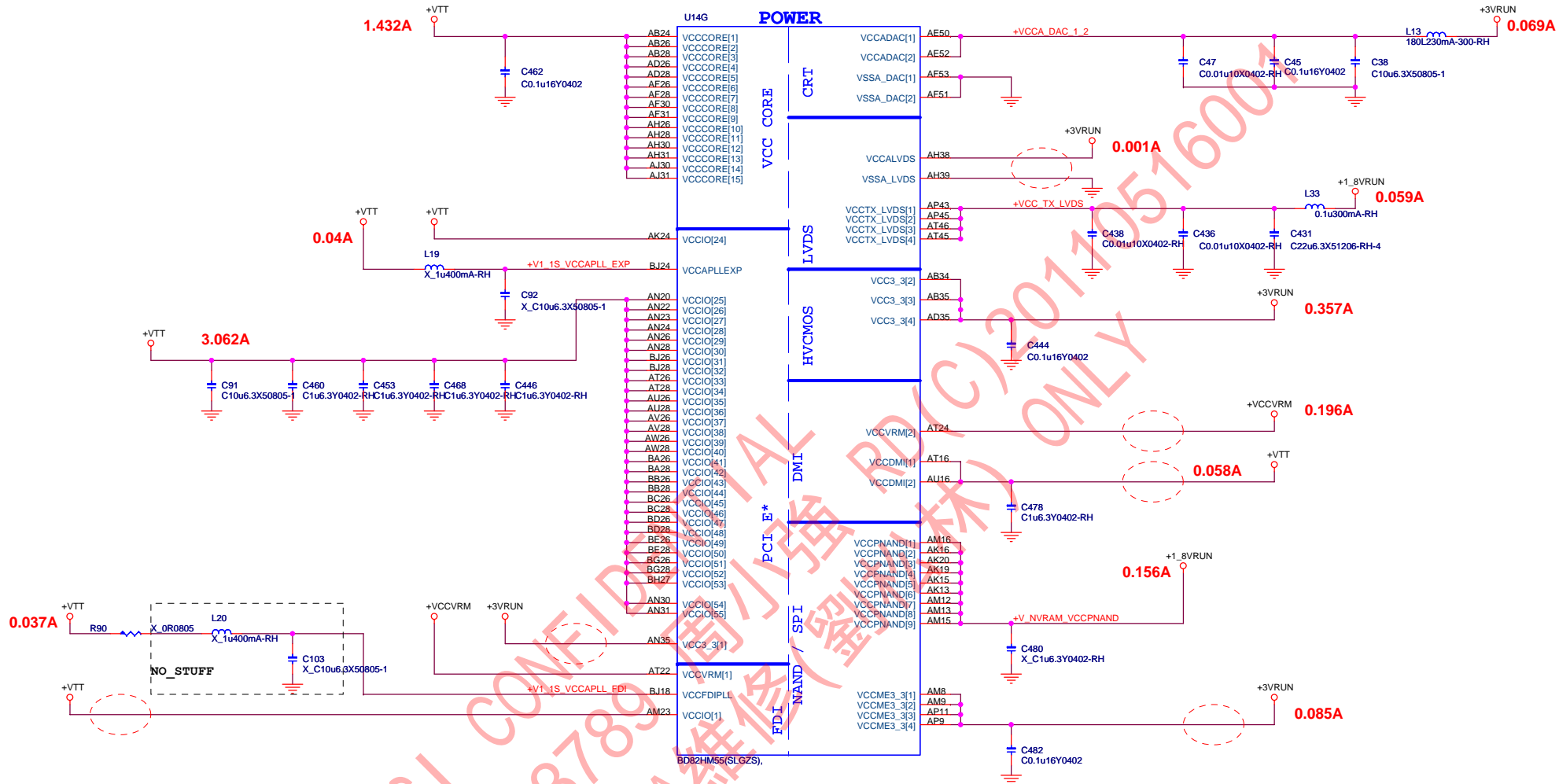
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

2009/06/26 For DGPU\_SELECT# driving reserved  
(No need for MS-1454)  
R367 not stuff for MS-1454

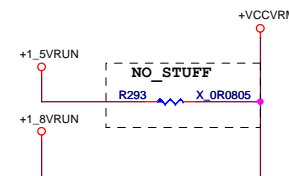




# IBEXPEAK - M (POWER)



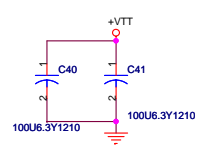
The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAC1k, Vccap11EXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.



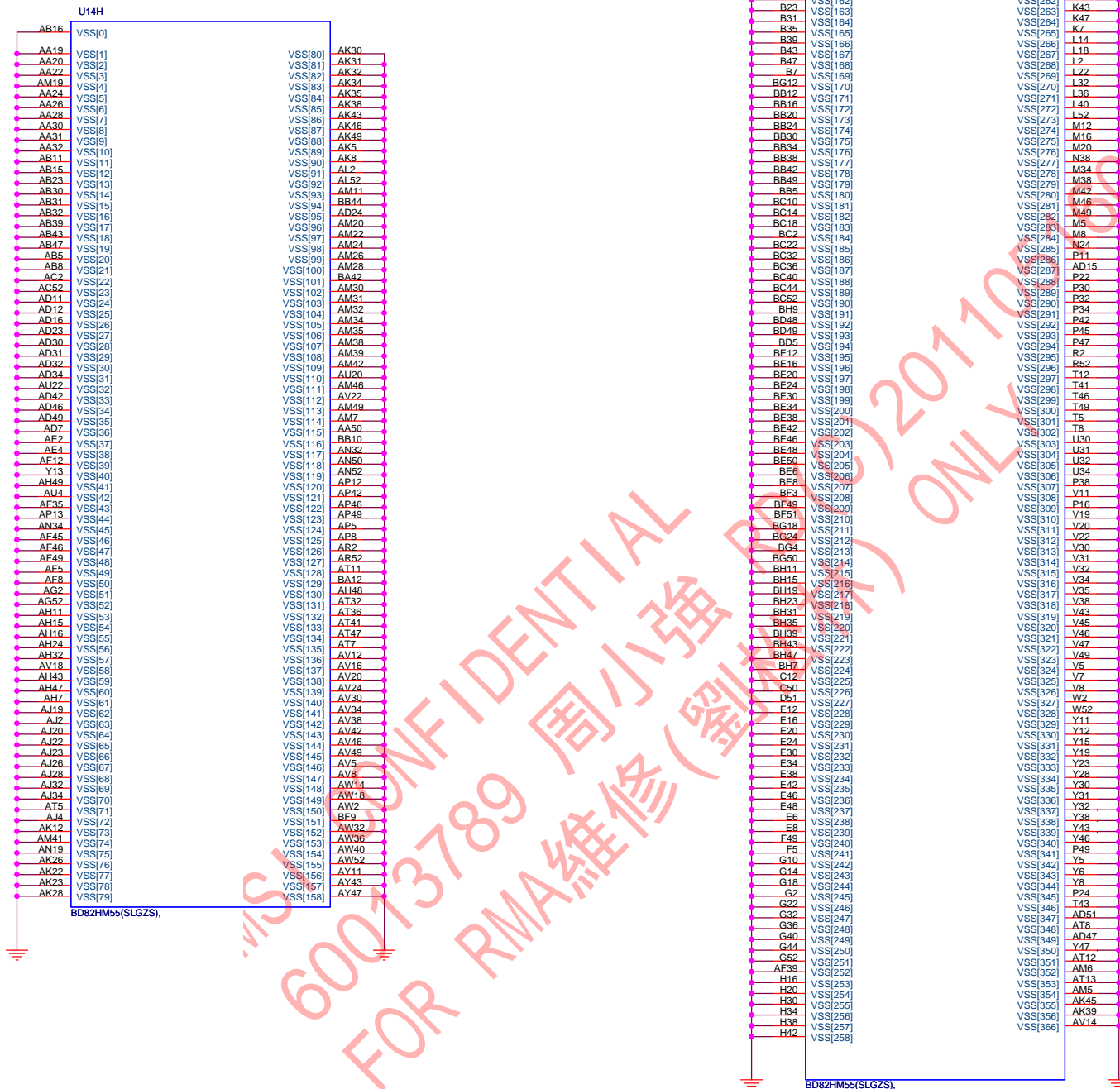
The schematic diagram illustrates the power and ground connections for the BD82HM56 (SLG25) microcontroller. The diagram is organized into several functional blocks, each with its own set of power and ground connections.

- USB:** This block includes connections for various USB pins, including VCCME[1] through VCCME[12], VCCIO[5], and VREF\_SUS. It shows connections to +3VSUS, +VTT, and +5VSUS rails.
- PCI/GPIO/LPC:** This block includes connections for VCC3\_3[8] through VCC3\_3[14], VCCIO[2] through VCCIO[4], and VCCSUS[2]. It shows connections to +V5A\_PCH\_VCCSREFSUS, +V5S\_PCH\_VCCSREF, +3VRUN, and +VTT rails.
- SATA:** This block includes connections for VCCSUS[3\_29] through VCCSUS[3\_32], VCCVIRM[4], VCCIO[9] through VCCIO[16], and VCCIO[17] through VCCIO[20]. It shows connections to +VCCVIRM, +VTT, and +3VSUS rails.
- CPU:** This block includes connections for V\_CPU\_IQ[1], V\_CPU\_IQ[2], and VCCRTC. It shows connections to +VTT and +3VSUS rails.
- HDA:** This block includes connections for VCCSUS[13] through VCCSUS[16]. It shows connections to +VTT and +3VSUS rails.

The diagram also shows various capacitors (C457, C470, C429, C442, C481, C135, C148, C463, C68) and a diode (D17) connected to different voltage rails. A large watermark "FOR IDENTIFICATION ONLY" is overlaid on the diagram.

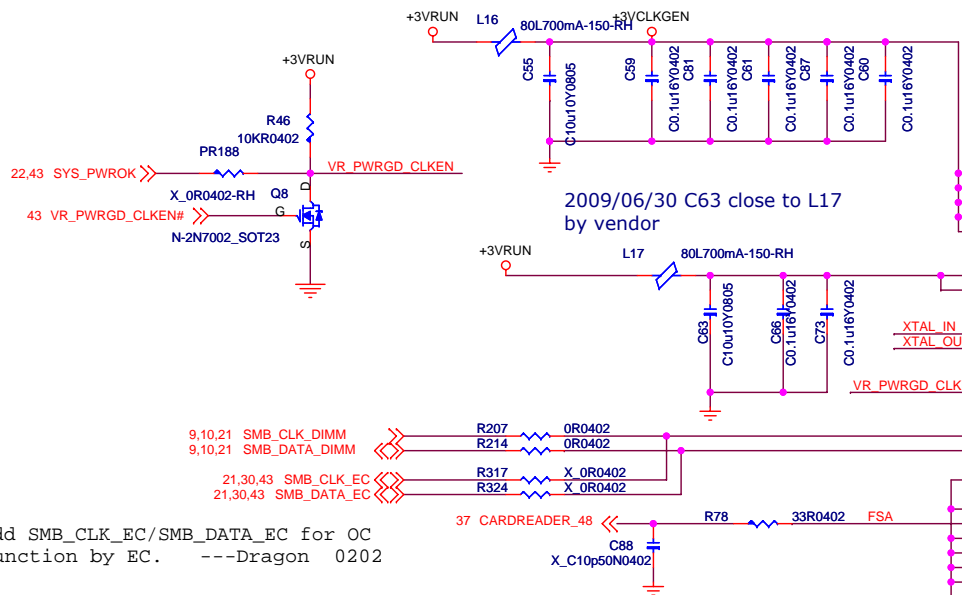


# IBEXPEAK - M (GND)





C59 Close to L16 ; C60,C61,C81,C87 Close to power pin



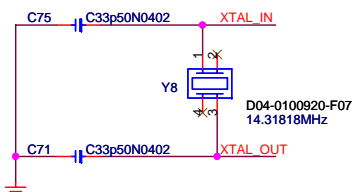
2009/06/30 C63 close to L17 by vendor

2009/06/22 Recommend 4.7KR or 10KR by vendor For Silego change to 2.2KR

To Park OSC Option

2009/07/08 Reserved for 0A test  
R3211 is for Spread clock(Default use)  
RB8 is for non-Spread clock

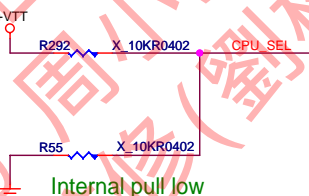
2009/07/08  
Y4传049S type(cost down as MS-1122)



Capacity select

If Cload=20pf C71/C75=33pf  
If Cload=32pf C71/C75=56pf

2009/06/30 R292 not stuff



Internal pull low

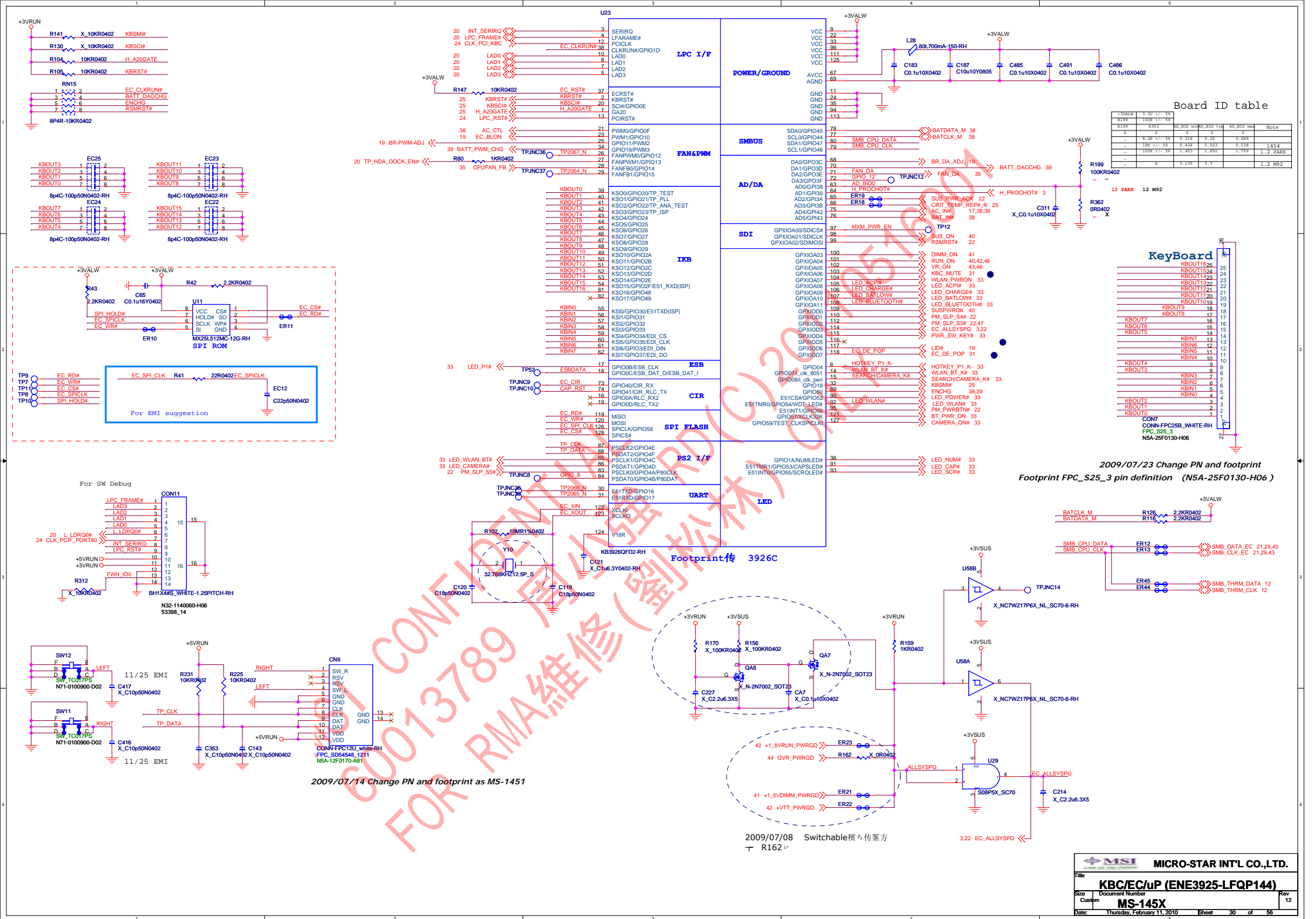
For CPU frequency select (133MHz)

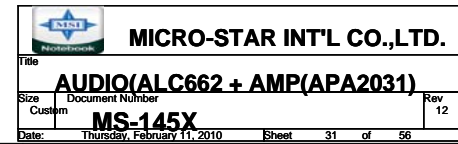
CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

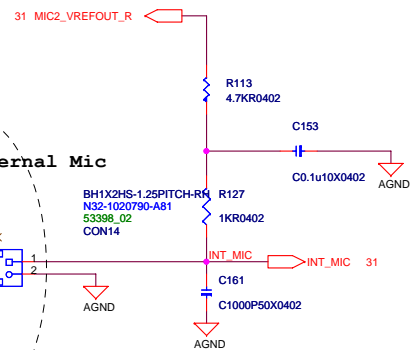
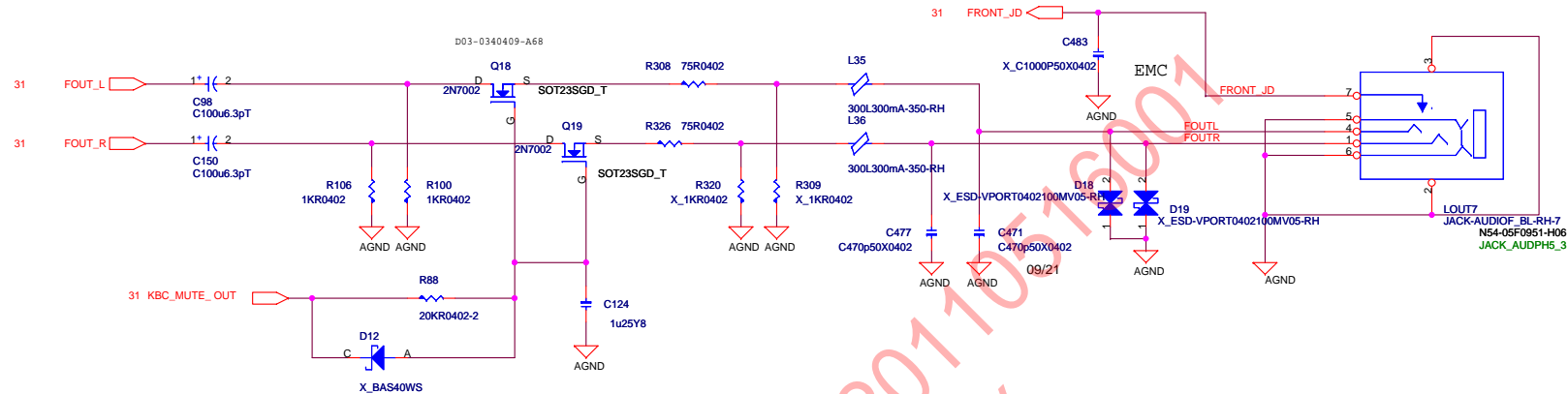
## Clock GEN. Vendor Table

	9LRS3199	SLG8SP587V
VDDIO spec	0.9975~3.465	1.05~3.466
BOM	R39 stuff	R40 stuff

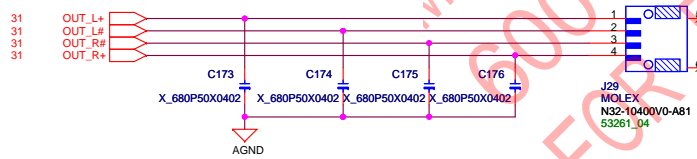
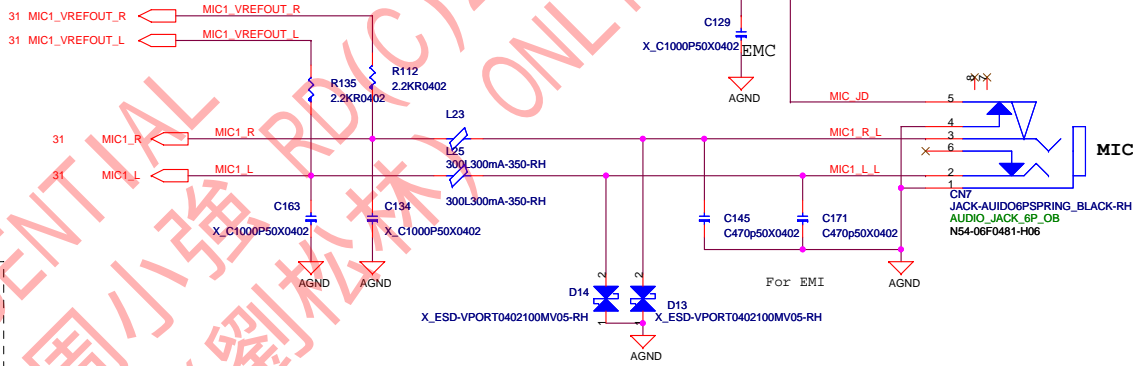
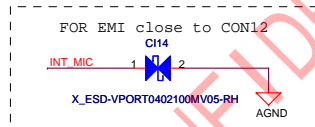


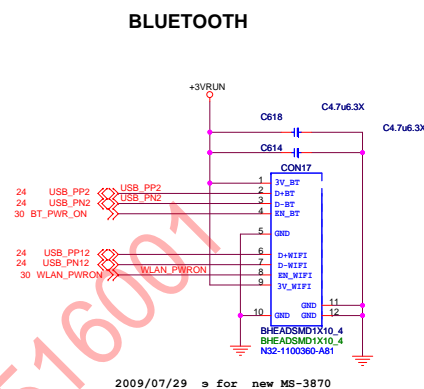
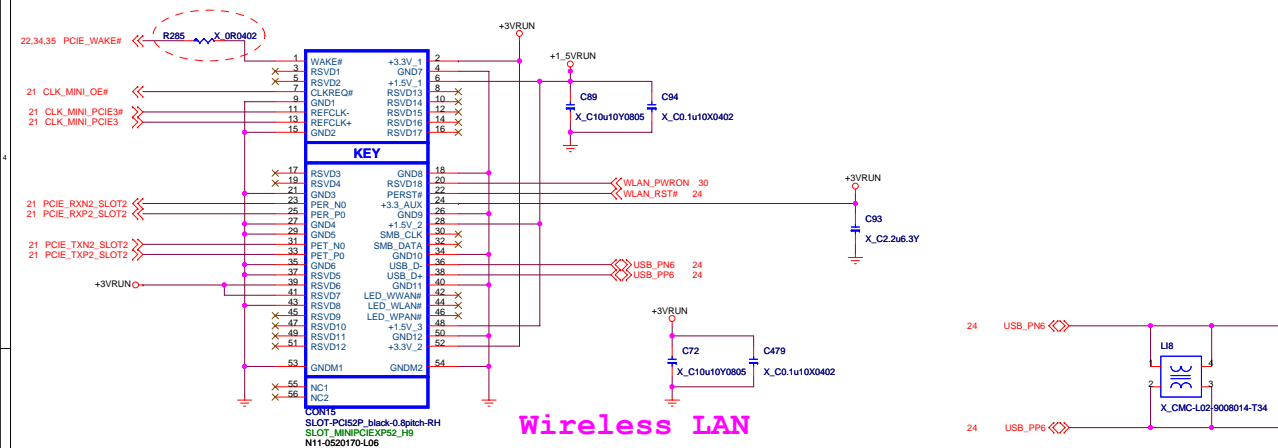






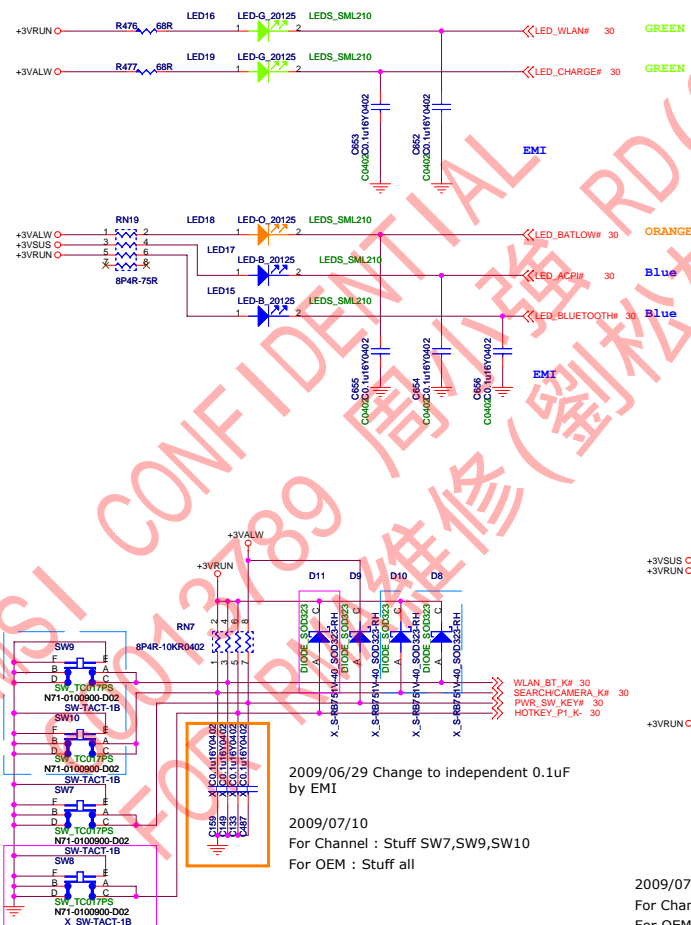
2009/06/29 Modify internal MIC PN to N32-1020790-A81





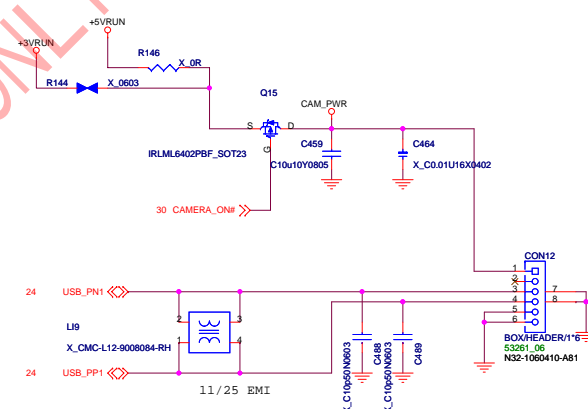
2009/07/29 3 for new MS-3870

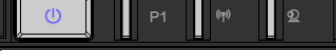
## LED light



**CAMERA**

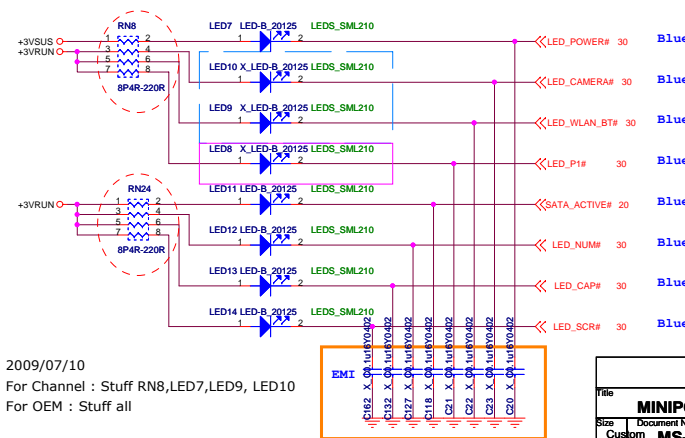
2009/06/29 Reserved 0 ohm pad  
by EMI



	LED7 SW7	LED8 SW8	LED9 SW9	LED10 SW10
				
1453	Stuff	Nostuff	Discreate	UMA
1454	Stuff	Nostuff	P1	IE
OEM	Stuff	P1	Wireless	Camera

## Stuff for CHANNEL

## Stuff for OEM

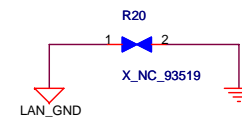
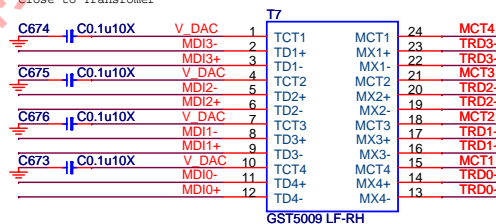
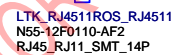
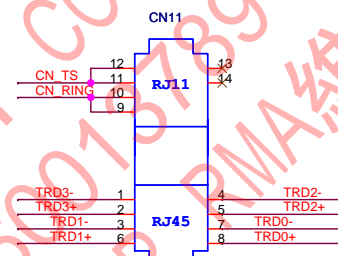
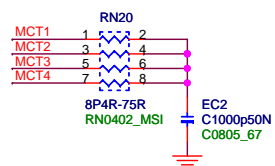
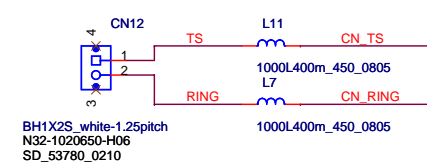
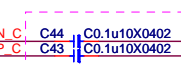
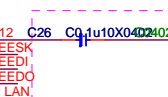
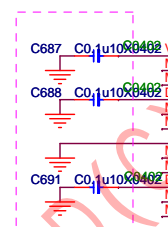
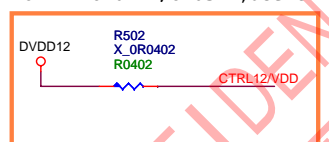
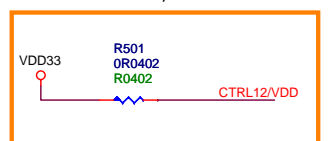
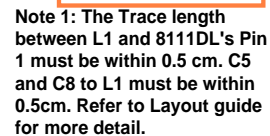
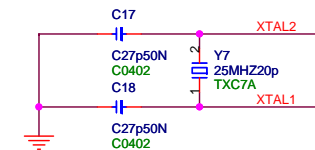
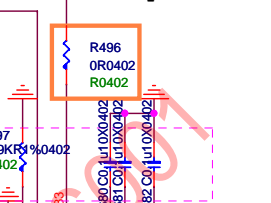
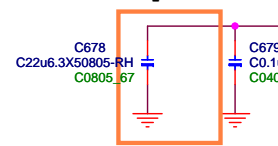
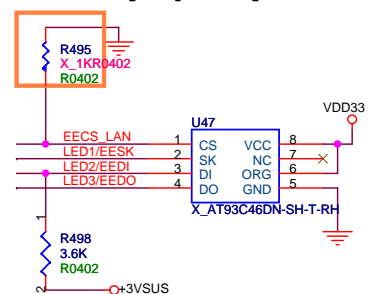
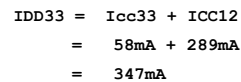


2009/07/10

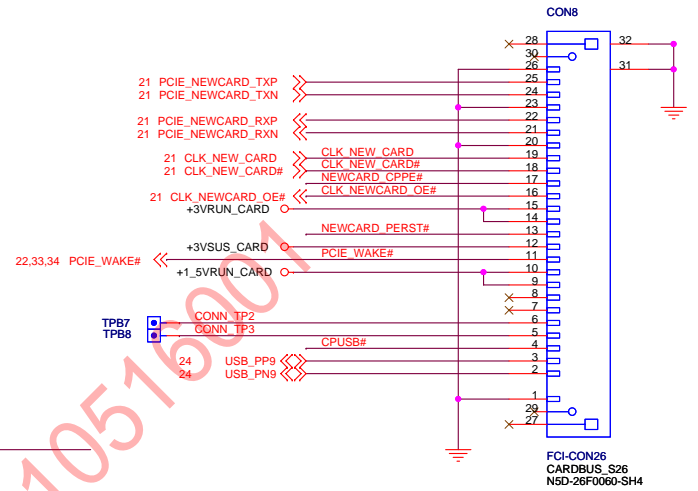
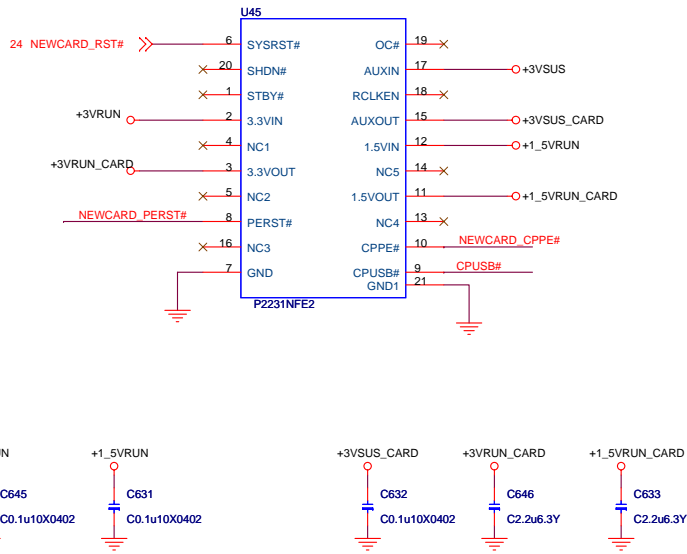
For Channel : Stuff RN8,LED7,LED9, LED10

For OEM : Stuff all

<b>MSI CORPORATION</b>			
Title <b>MINIPCIE,CAMERA,BLUETOOTH,SW</b>			
Size	Document Number		Rev
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NEW CARD

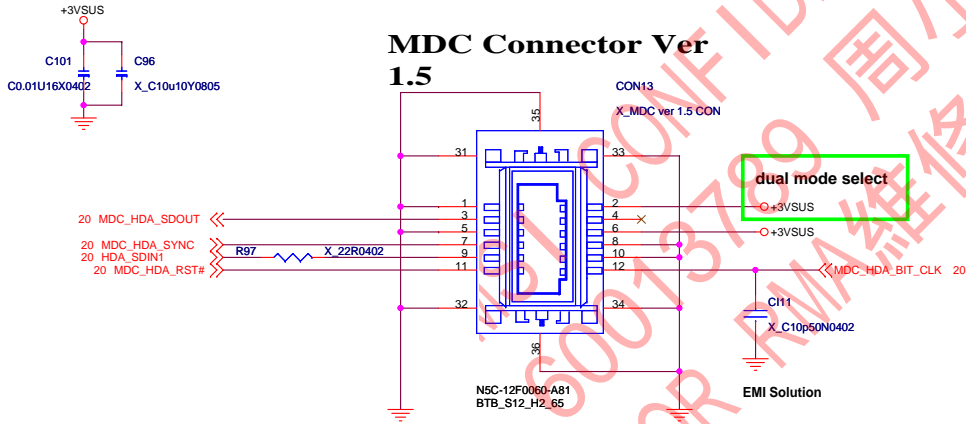


2009/06/26 Reserved by EMI

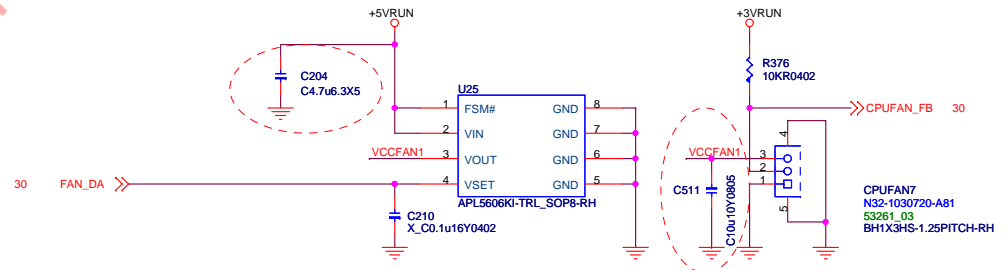
MDC Connector

MDC 1453 NO STUFF; 1454 STUFF!

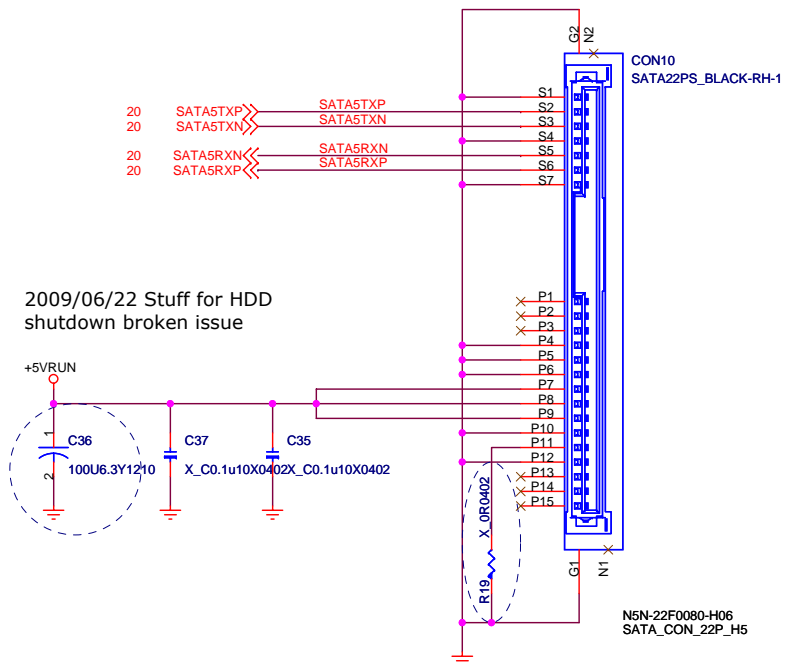
MDC Connector Ver 1.5



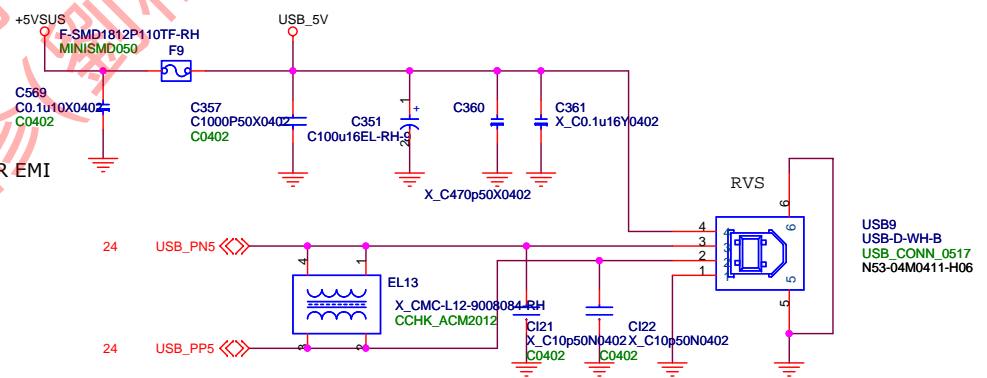
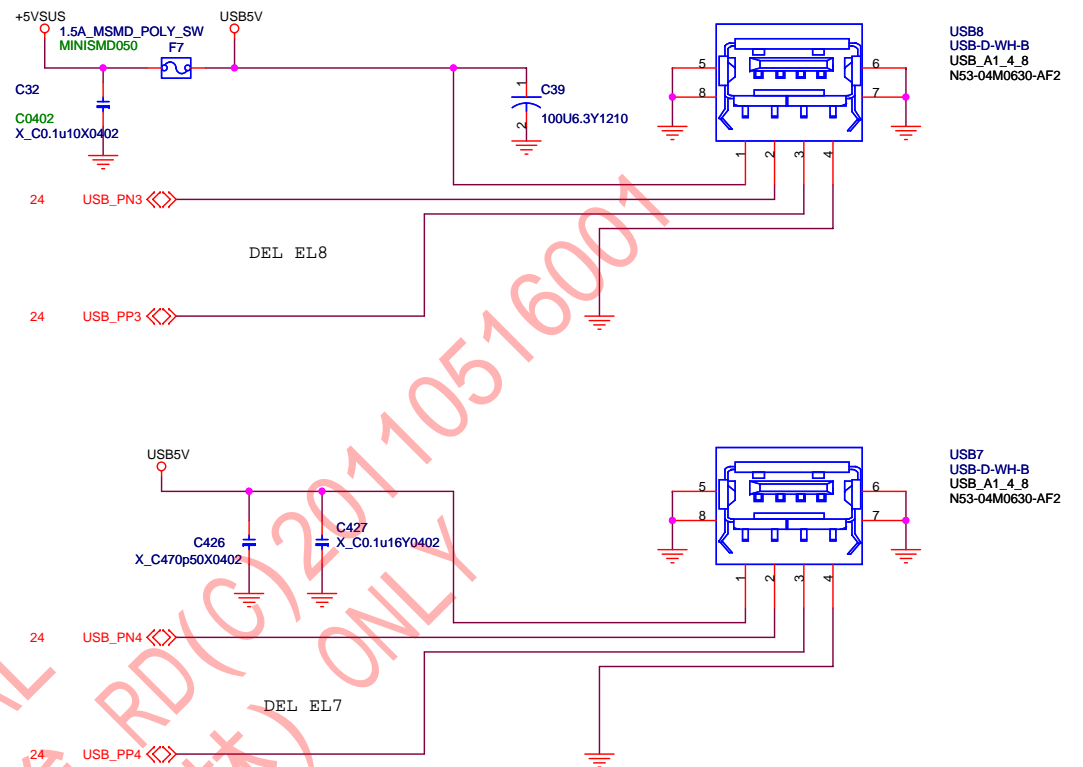
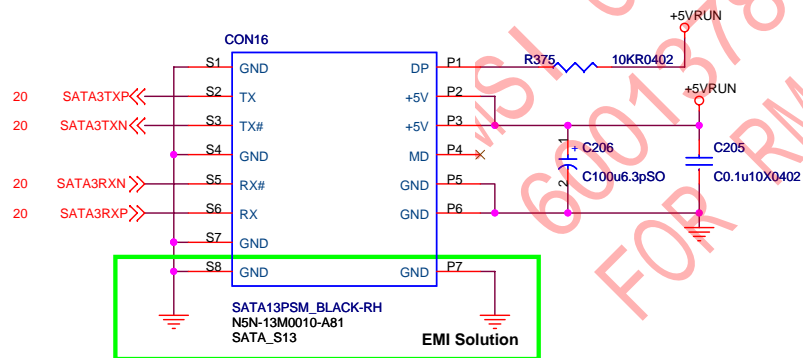
CPU FAN



## SATA HDD



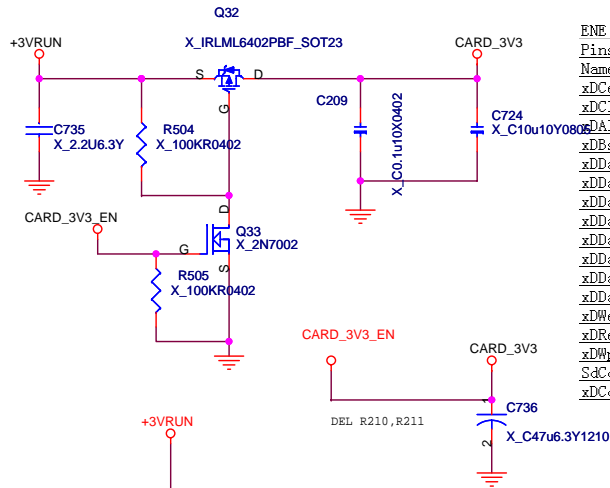
## SATA ODD



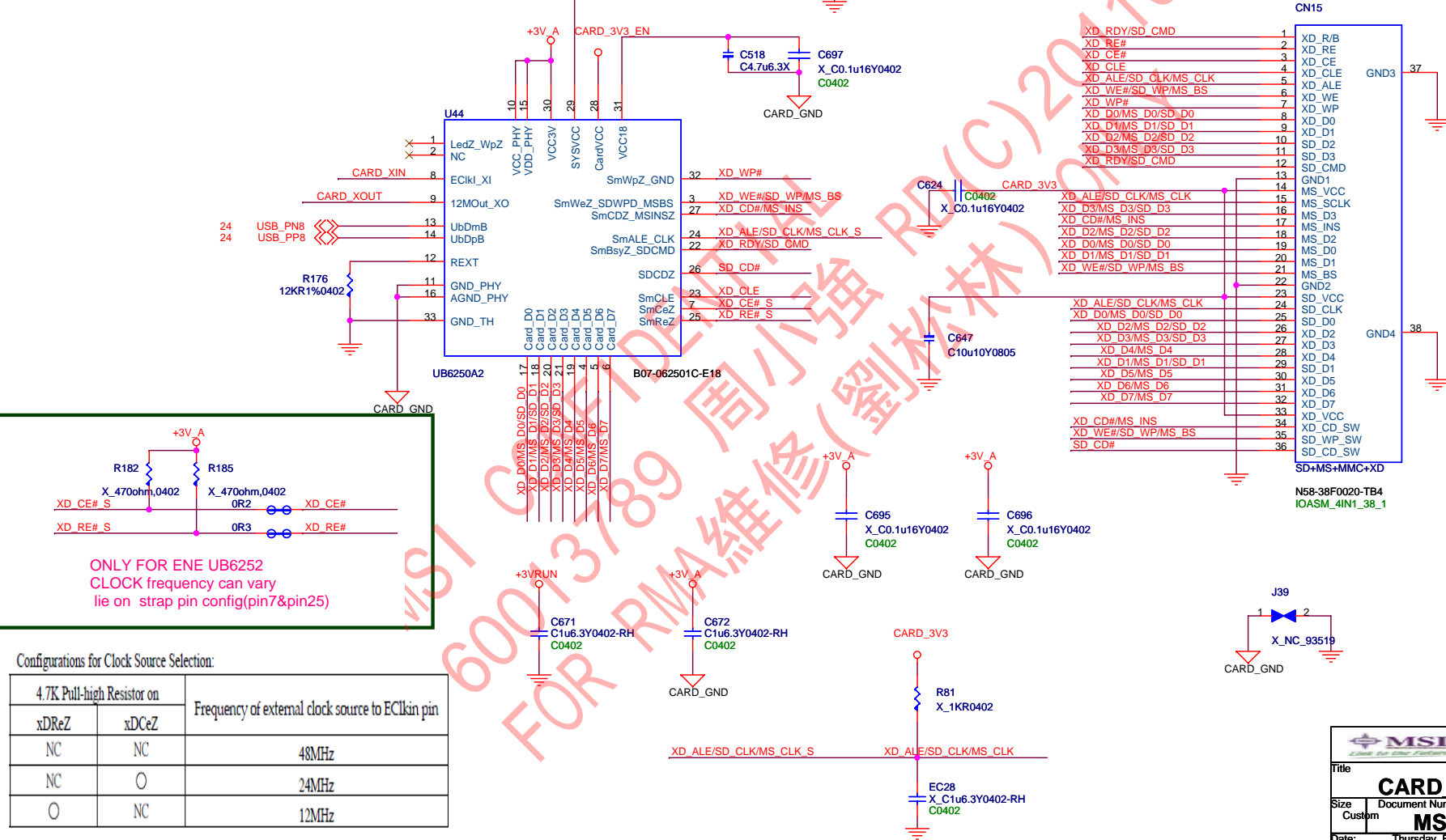


29 CARDREADER\_48 >>> R473 CARD\_XIN

2009/07/01 48MHz from Clock GEN.



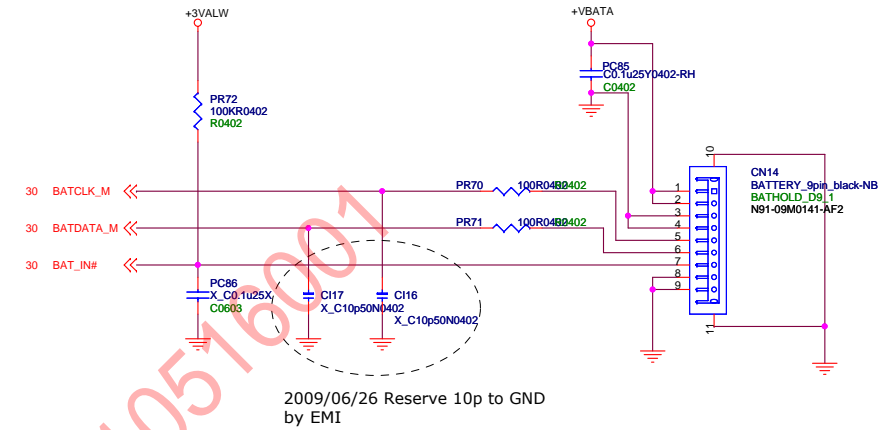
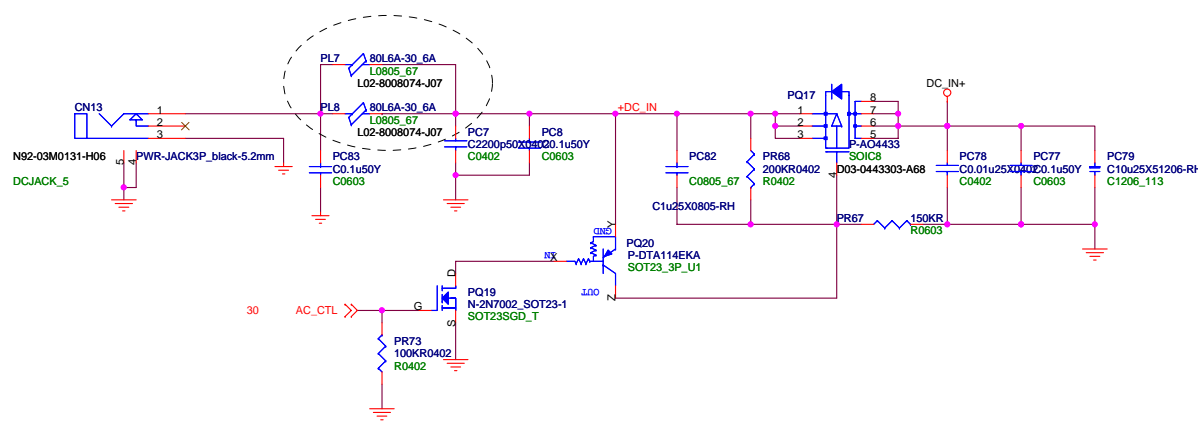
ENE UB6250 USB20 Flash Card Reader Controller									
Pins for SD, MMC, MS, and xD memory cards									
Name	No	I/O	XD	SD	MMC	MS			
xDCE#	7	O	xD card EN						
xDCl#	23	O	xD CMD latch EN						
xDAl#	24	O	xD ADDR latch EN	SD clock	MMC clock	MS serial clock			
xD#	22	B	xD Ready/busy	SD CMD/response	MMC CMD/response				
xDData0	17	B	xD D0	SD D0	MMC D0	MS D0			
xDData1	18	B	xD D1	SD D1	MMC D1	MS D1			
xDData2	20	B	xD D2	SD D2	MMC D2	MS D2			
xDData3	21	B	xD D3	SD D3	MMC D3	MS D3			
xDData4	19	B	xD D4		MMC D4	MS D4			
xDData5	4	B	xD D5		MMC D5	MS D5			
xDData6	5	B	xD D6		MMC D6	MS D6			
xDData7	6	B	xD D7		MMC D7	MS D7			
xDWe#	3	B	xD W EN	SD WP					
xDRe#	25	O	xD R EN						
xDWp#	32	O	xD WP						
SDCd#	26	I		SD CD	MMC CD				
xDc#	27	I	xD CD			MS CD			



Configurations for Clock Source Selection:

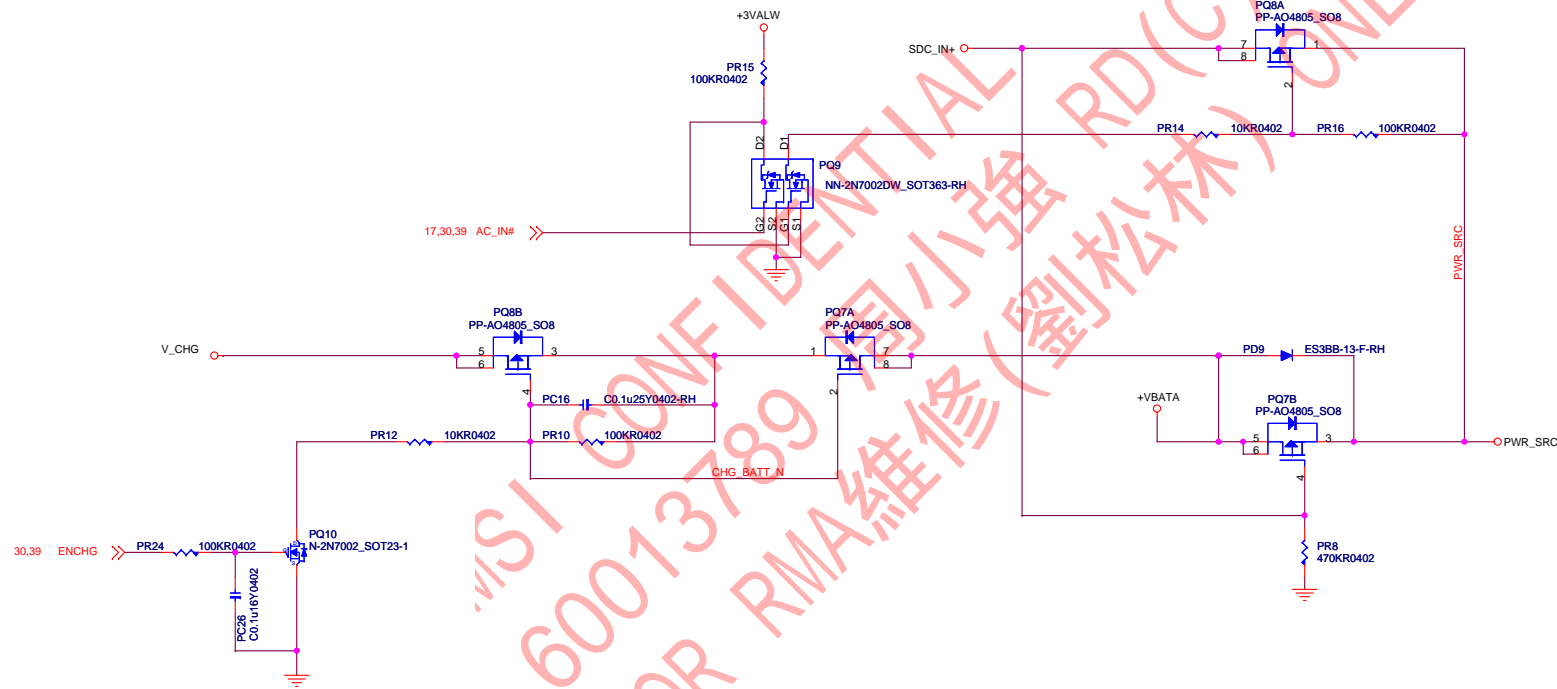
4.7K Pull-high Resistor on		Frequency of external clock source to EC1kin pin
xDRe#	xDCE#	
NC	NC	48MHz
NC	O	24MHz
O	NC	12MHz

2009/07/10 65W adaptor 惠璵 BEAD



# JBAT1 Pin Definition

- 1: VBATA+
- 2: VBATA+
- 3: NC
- 4: NC
- 5: SMBCLK
- 6: SMBDATA
- 7: BAT\_IN#
- 8: GND
- 9: GND

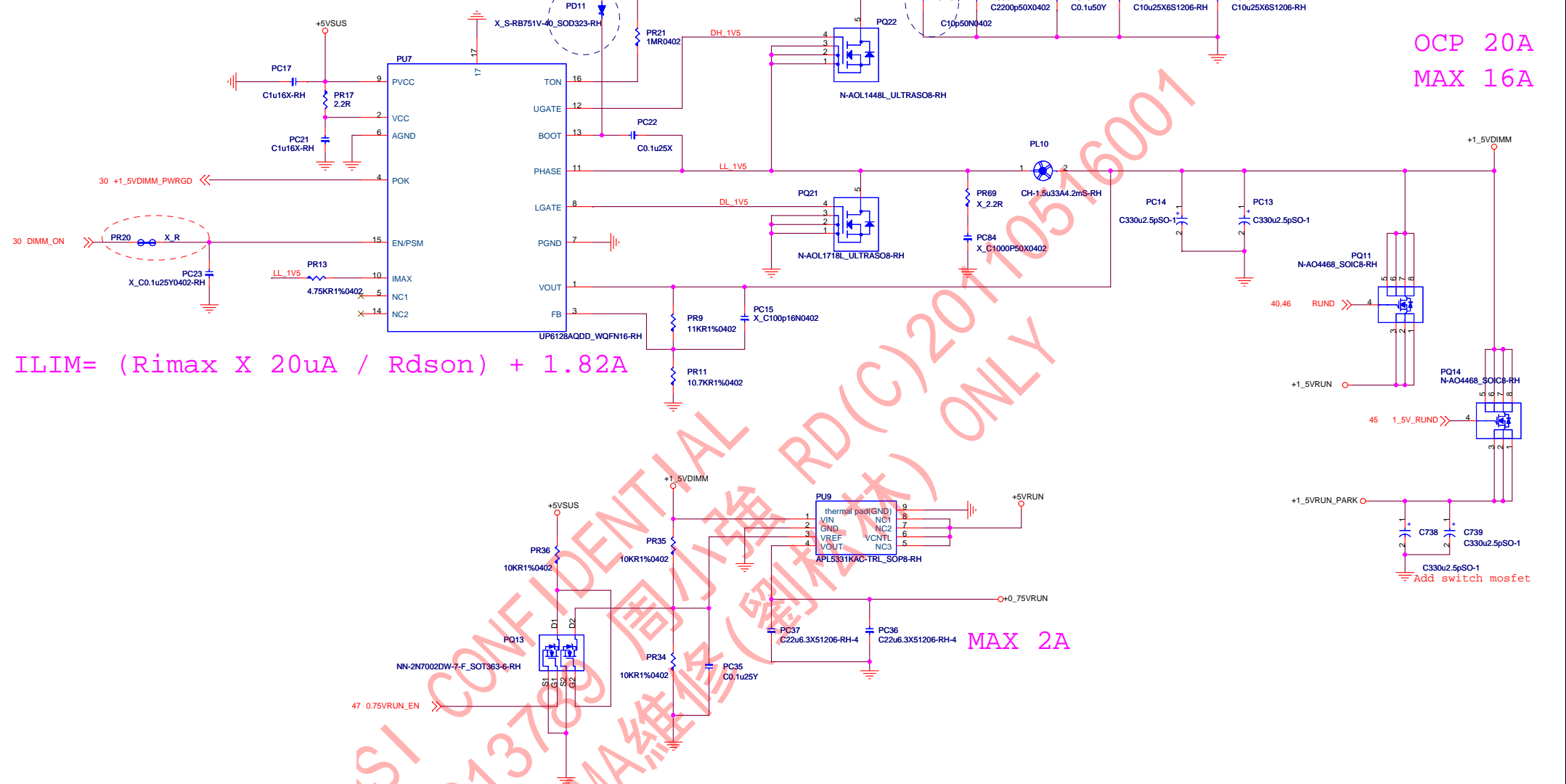






2009/07/10 轟と 瞬ノ

2009/06/26 Reserve 10p to GND  
by EMI (Close to PQ21)



OCP 20A  
MAX 16A

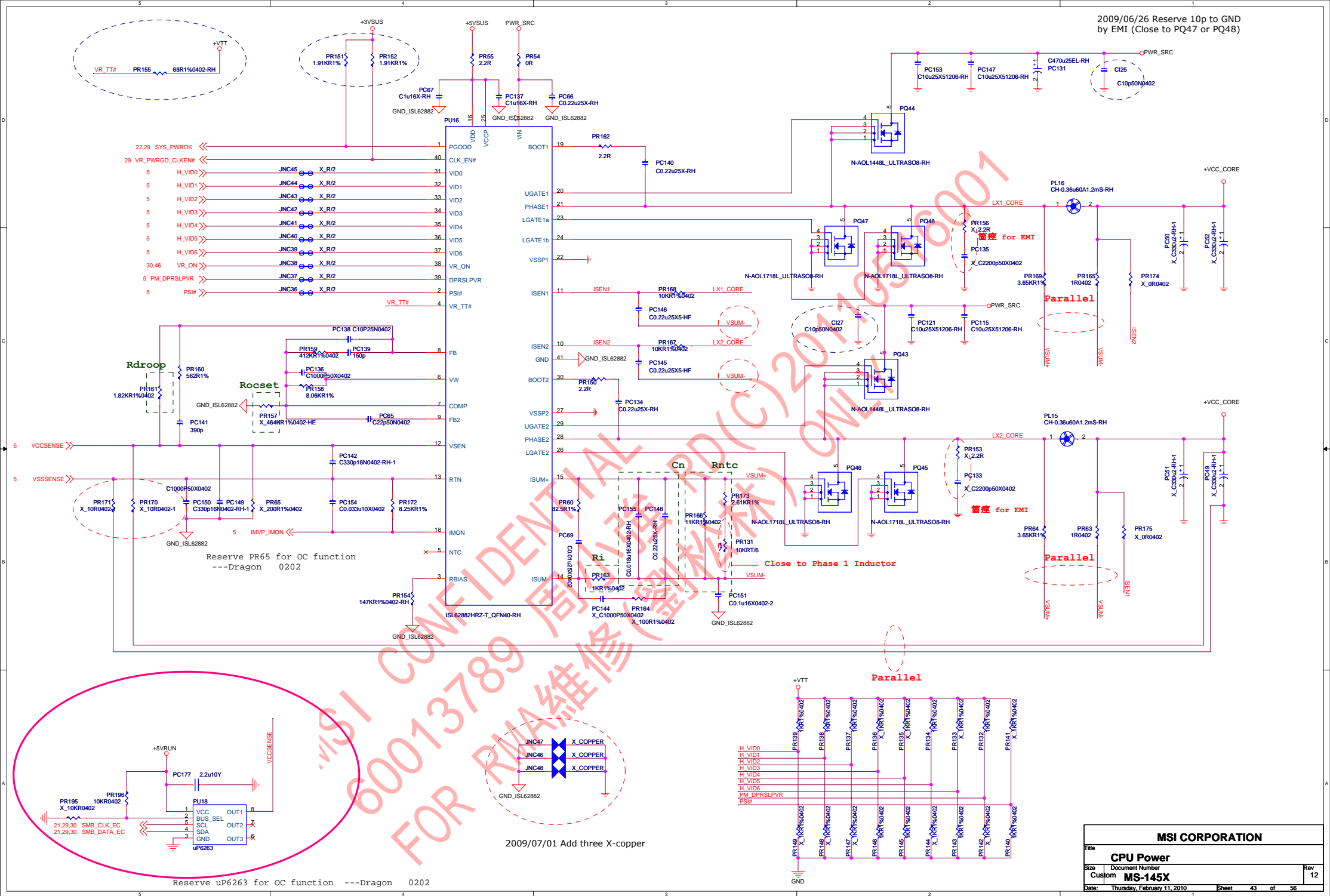
$$ILIM = (R_{imax} \times 20\mu A / R_{dson}) + 1.82A$$

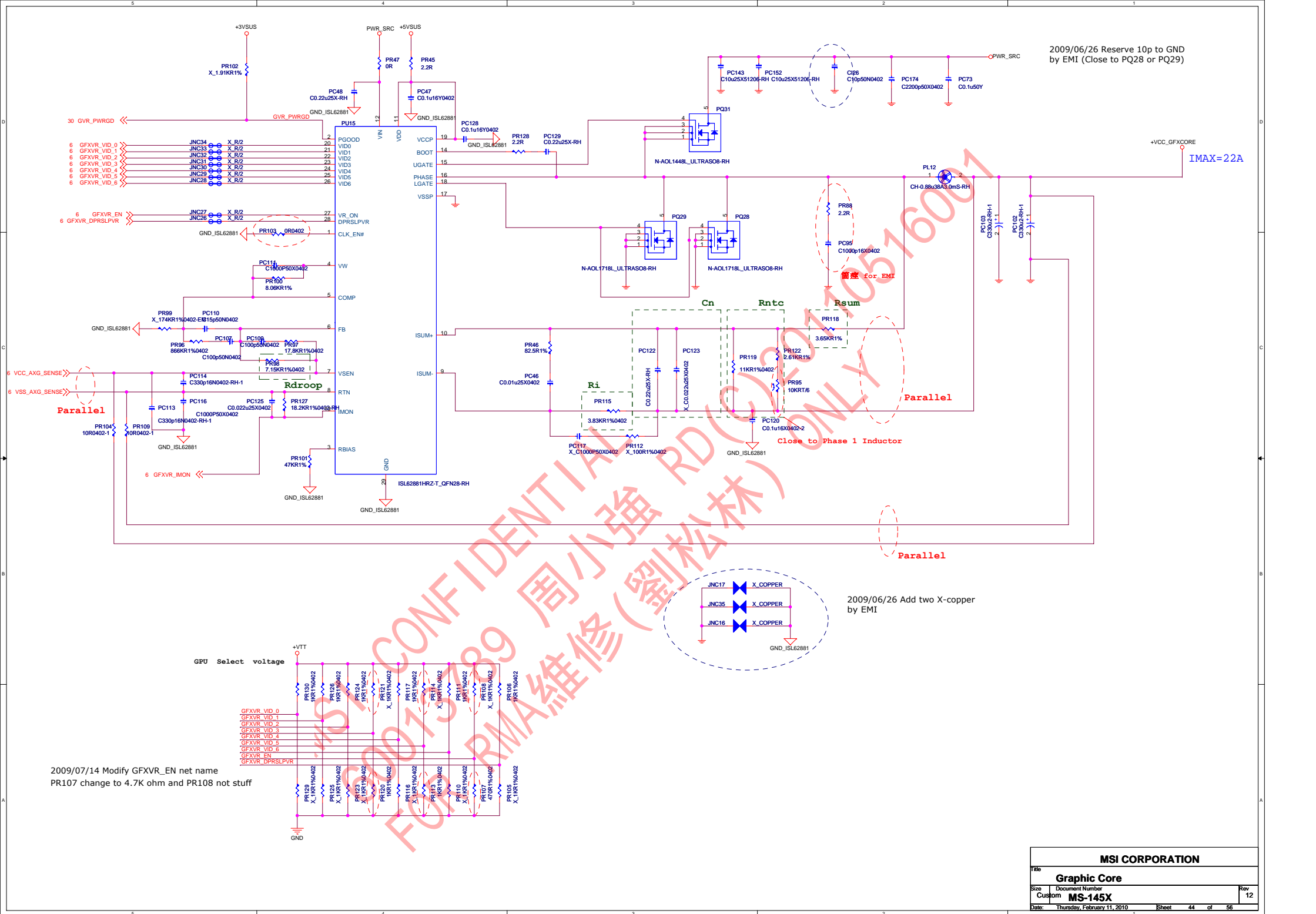
MAX 2A



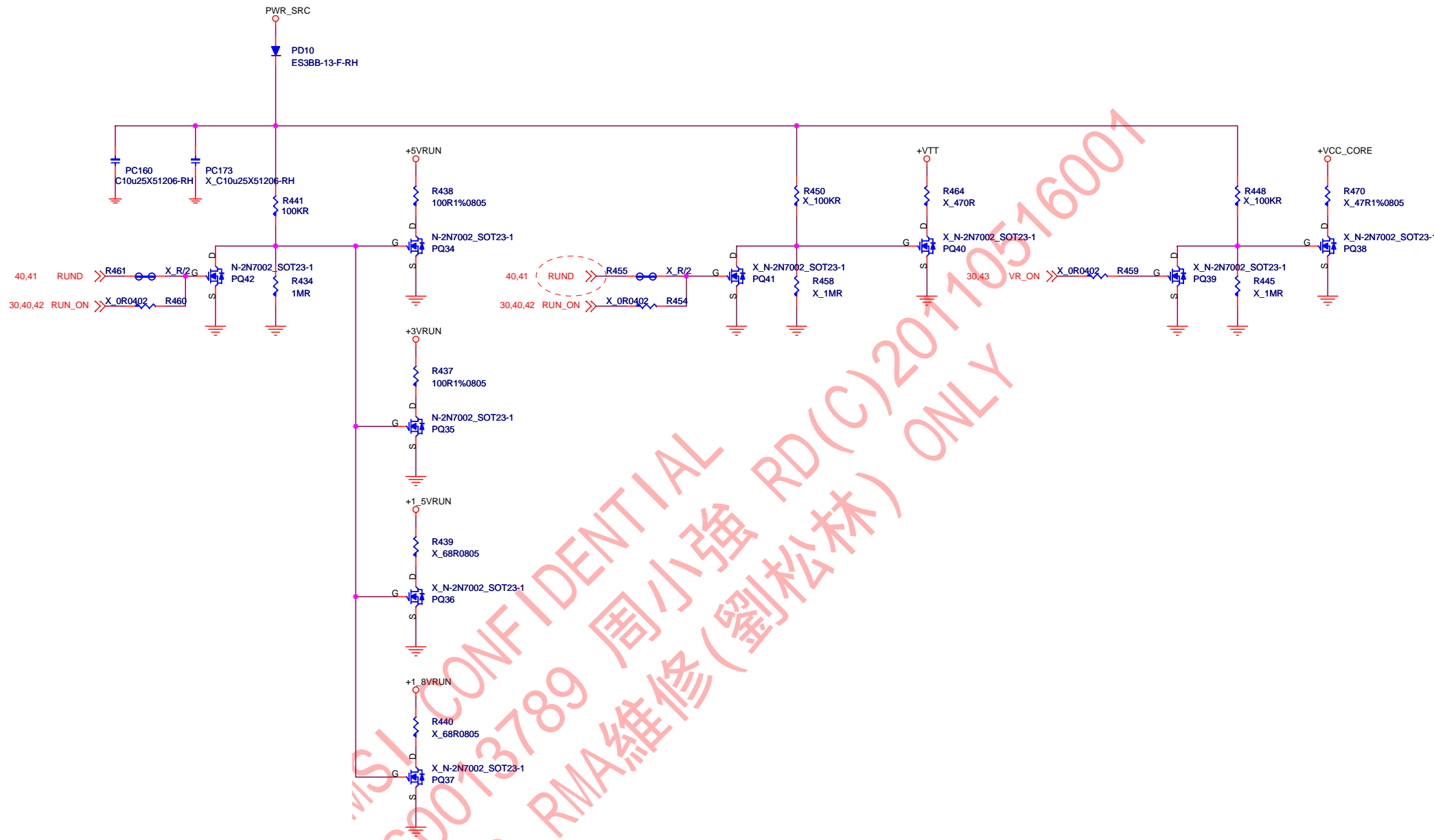


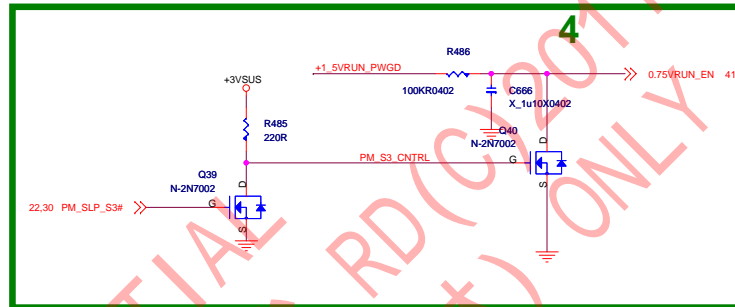
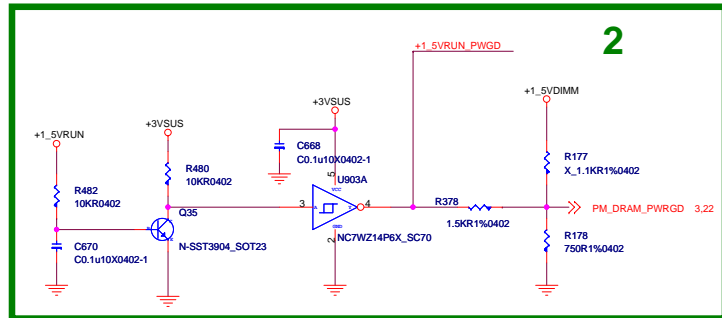
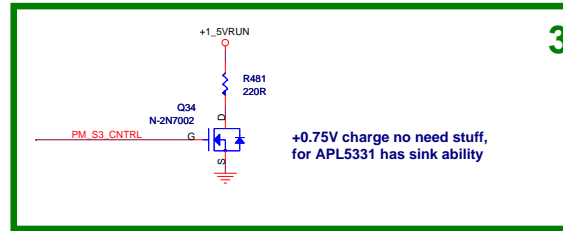
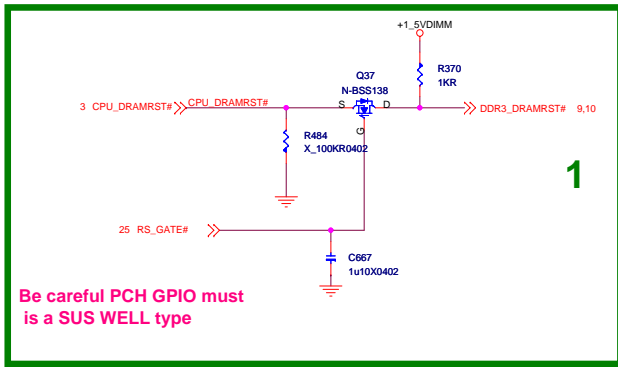
<b>MSI CORPORATION</b>			
Title			
<b>CPU Power</b>			
Size	Document Number		Rev
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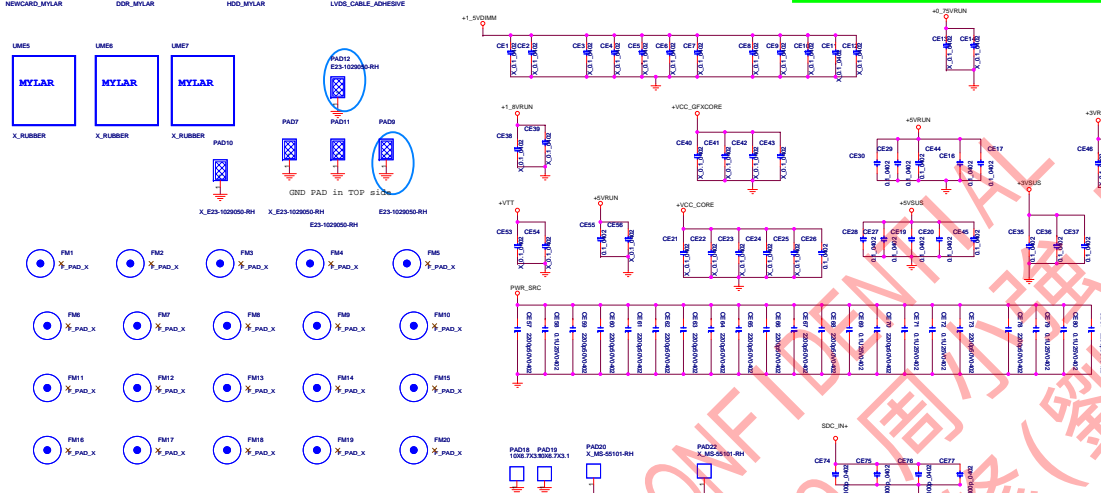






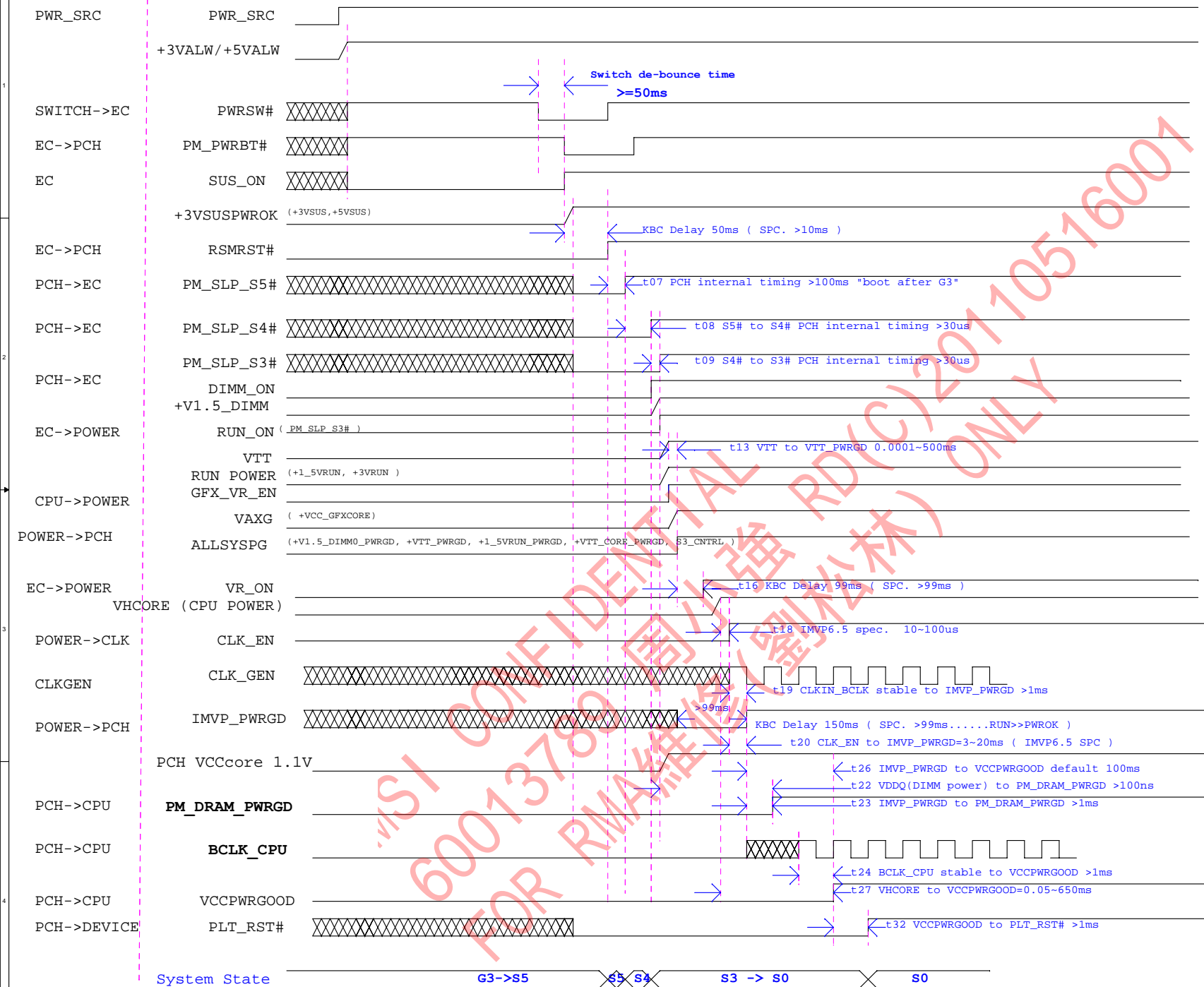




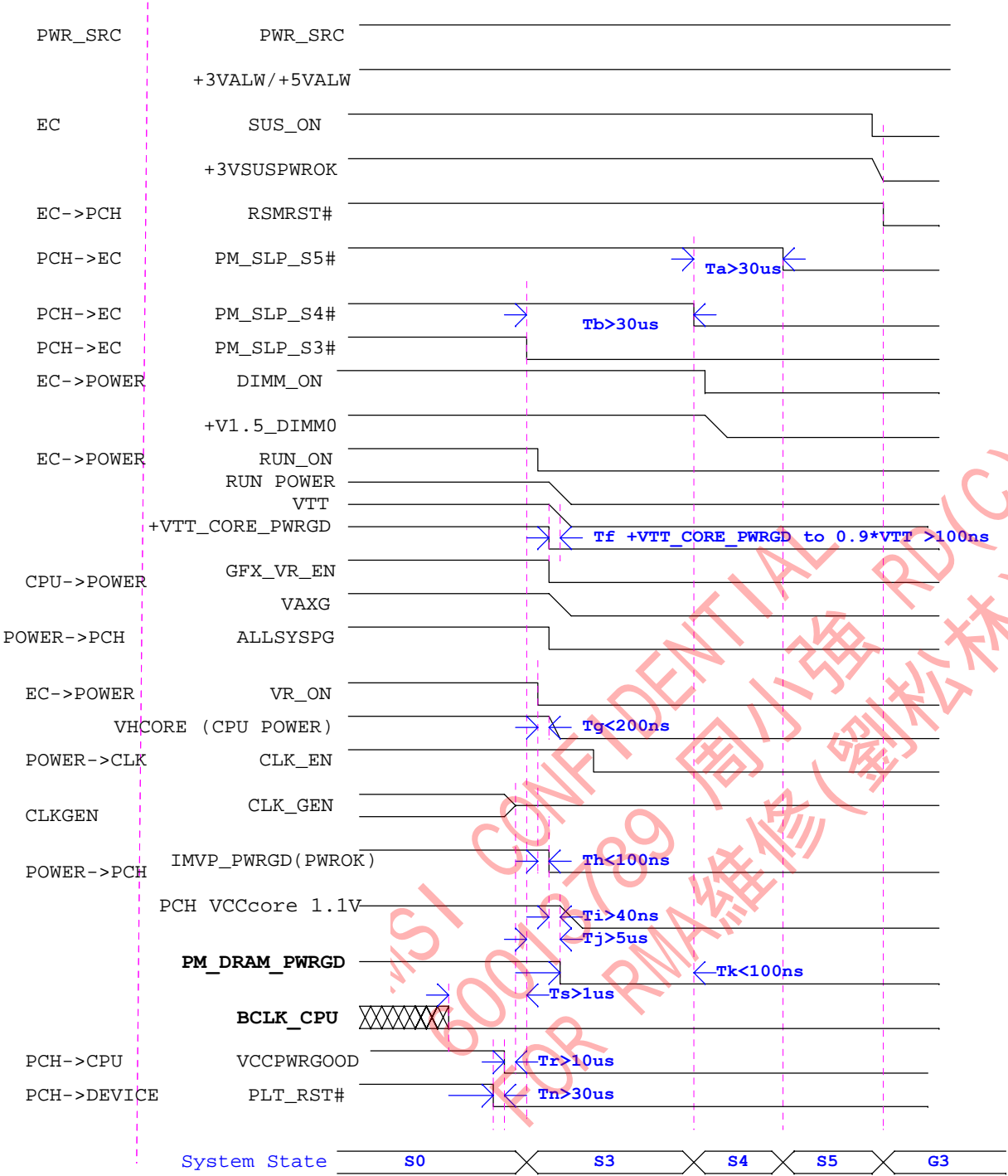
[illegible]



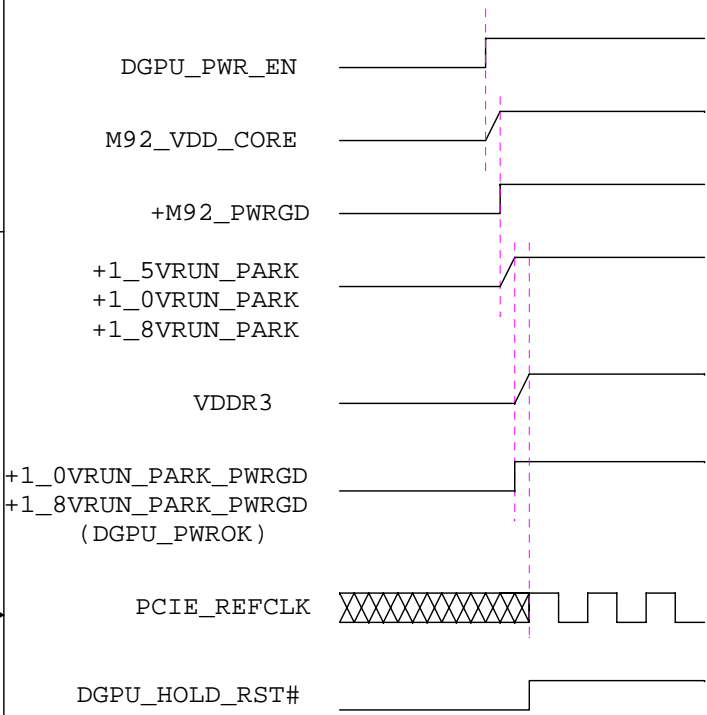
## Calpella System Power on Sequence DC mode



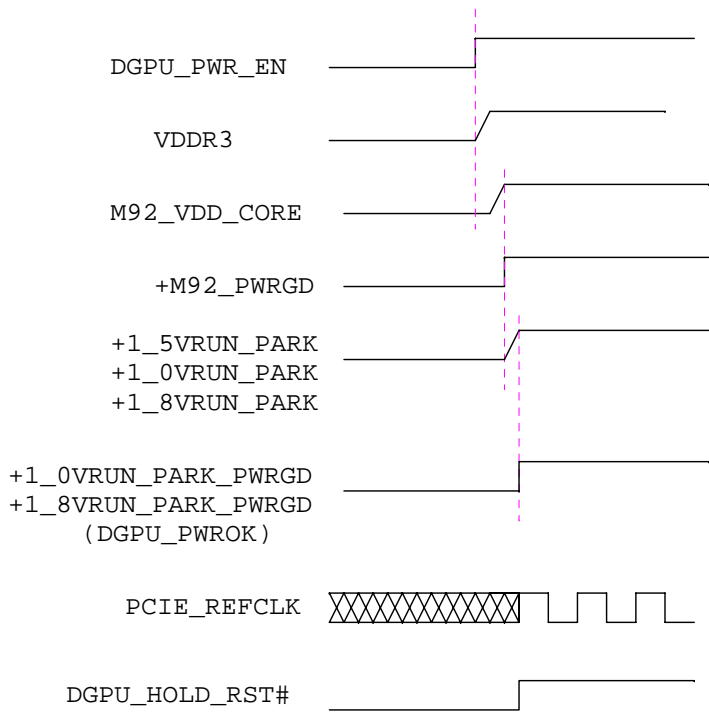
Power down Sequence DC mode S0 to G3



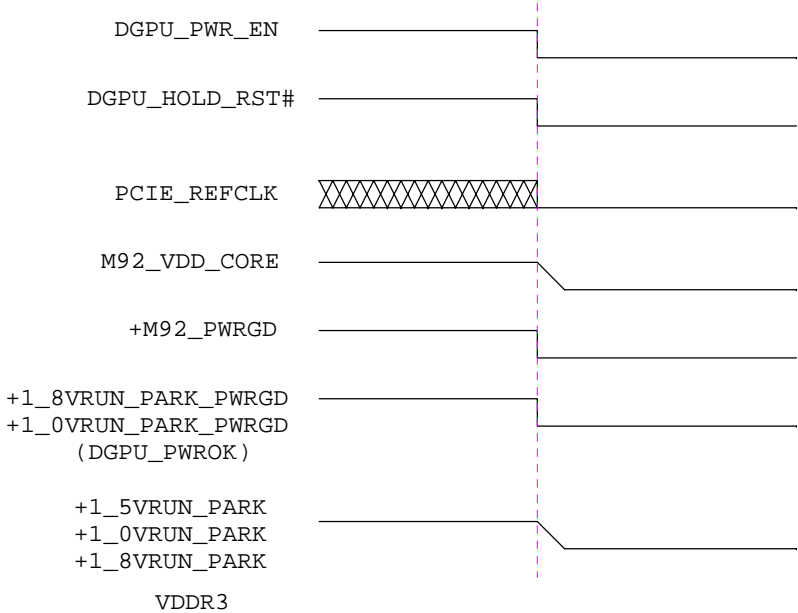
M92 Power on Sequence



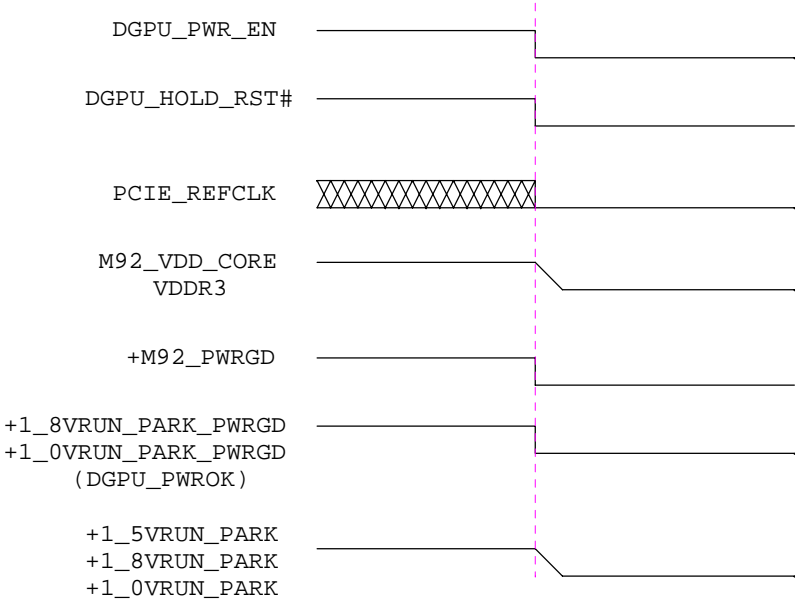
PARK Power on Sequence



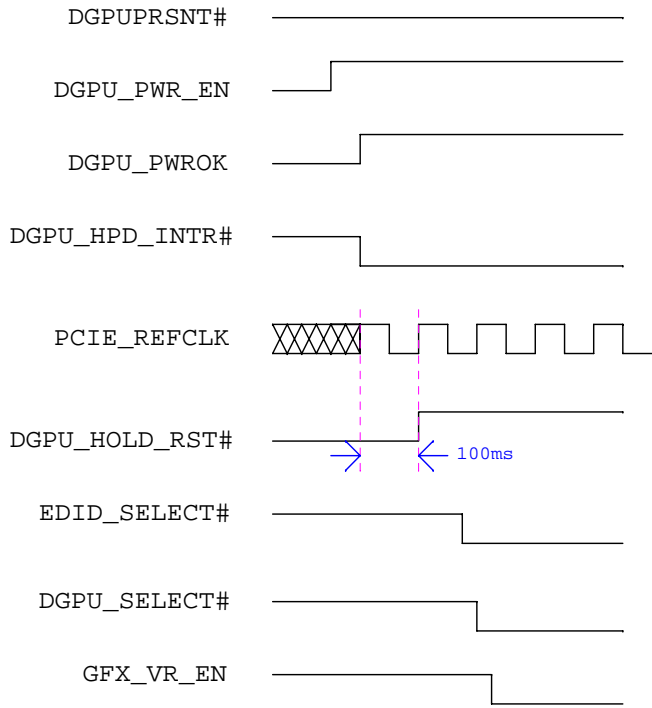
M92 Power down Sequence



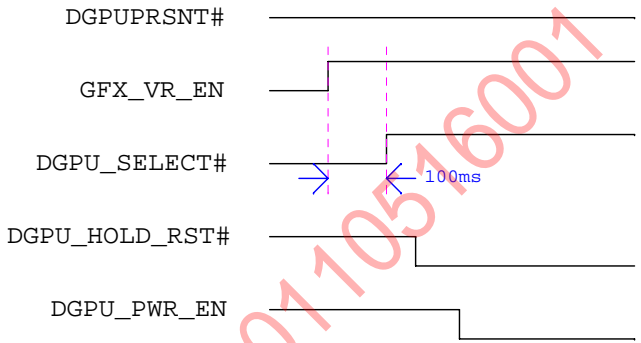
PARK Power down Sequence



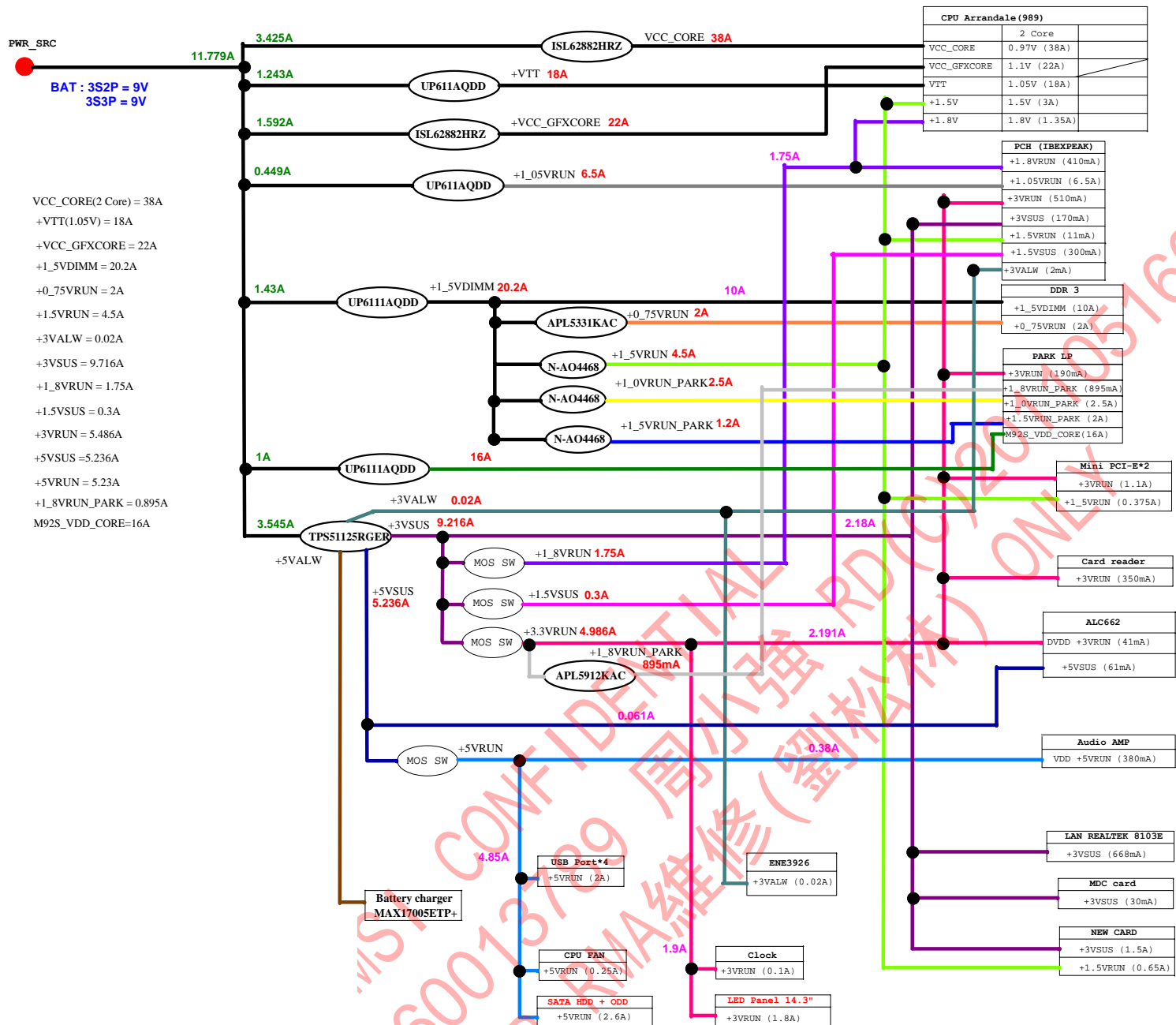
Switchable DGPU Power on Sequence  
Discrete Mode



Switchable DGPU Power off Sequence  
UMA Mode



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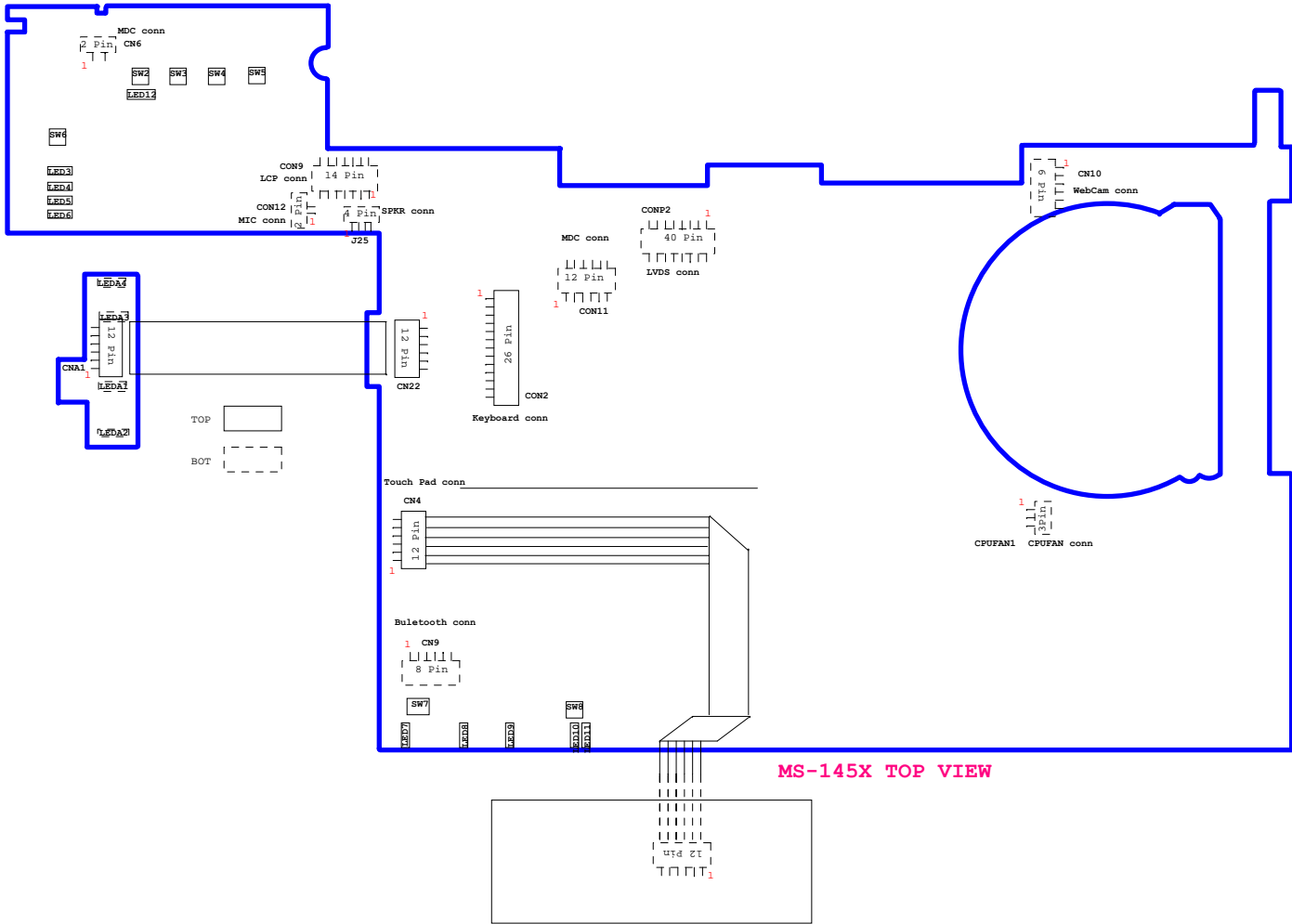


MS-145X	
SW2	Power_button(FOR OEM)
SW3	HotKeyF1_button( FOR OEM)
SW4	WLAN/BT_button(FOR OEM)
SW5	Search/Webcam_button (FOR OEM)
SW6	Power_button(FOR Channel)
SW7	Right_button
SW8	Left_button

MS-145X	
LED3	HDD_LED (FOR OEM)
LED4	NUM_LED ( FOR OEM)
LED5	CAP_LED (FOR OEM)
LED6	SCR_LED (FOR OEM)
LED7	BT_LED
LED8	WLAN_LED
LED9	ACPI_LED
LED10	CHARGE_LED
LED11	BATTERY_LOW_LED
LED12	POWER_LED

MS-145XA	
LEDA1	NUM_LED (FOR OEM)
LEDA2	HDD_LED ( FOR OEM)
LEDA3	CAP_LED (FOR OEM)
LEDA4	SCR_LED (FOR OEM)

MS-145X : Main Board  
MS-145XA : LED board



MS-145X TOP VIEW

2009/06/25 [Page33] Add LED and switch function for OEM reserved  
[Page30] Delete KBOUT16,KBOUT17 for MS-1451 keyboard matrix  
[Page41/42] Modify APL5912 VCNTL to +5VSUS  
[Page43/44] Modify some RC footprint and value

2009/06/26 Modify circuit to Switchable

[Page19] Add LVDS common choke by EMI

[Page12] Reserve RGB 10p to GND

[Page38] Reserve BAT CLK and DATA 10p to GND

[Page39] Reserve 10p SDC\_IN+ to GND and close to PQ57  
Add two X-Copper

[Page40] Reserve 10p +5VSUS to GND and close to PQ60  
Reserve 2.2R+2200p

[Page41] Reserve 10p PWR\_SRC to GND and close to PQ68

[Page42] Reserve 10p PWR\_SRC to GND and close to PQ72

[Page43] Reserve 10p PWR\_SRC to GND and close to PQ75 or PQ76  
Reserve 10p PWR\_SRC to GND and close to PQ78 or PQ79

[Page43] Reserve 10p PWR\_SRC to GND and close to PQ81 or PQ82  
Add two X-Copper

2009/06/29 [Page35] Modify CPU FAN.Add C121 and C304 by datasheet.Add one more RC for FAN speed calculation(as MS-1122)  
Modify PARK circuit  
Modify PCH PN to OB1-1675001 for Mobile IntelR 5 Series Chipset Full Feature  
Modify Audio jack PN to N54-05F0951-H06  
Modify internal MIC PN to N32-1020790-A81  
Modify power sequence map

2009/07/01 [Page3] R234,R412単0A龟喷嘴挡栅 / ) 瑛 瑛埃  
BPM#[0~7] remove  
BCLK 痾痾from PCH,瑛埃from CLOCK GEN.

[Page5] Short bead

[Page6] Short bead

[Page7] VSS\_NCTF1~7 remove

[Page8] 獬廌CFG 代獬,尤縑簿埃

[Page9] SA0\_DIM0のSA1\_DIM0は 0 ohm  
 330uF, CPU のswitching power

[Page10] SA0\_DIM1a 0 ohm癸  
簿埃330uF, CPU のswitching power狼 T

[Page12] 干 HPD結隔

[Page16] MDA0~MDA7 swap

[Page18] CRT の LVDS 簡短条 (for MS-1454)A<sub>3</sub> 虫登 0 ohm  
EDID switch 条方 pin 0.1uF  
R3238,R3239<sub>3</sub> 10K ohm  
薄埃 BR-AD-ADJ,BR-PWM-ADJ 嘿<sub>3</sub> PWM-ADJ,HDMI DDC 嘿<sub>3</sub> HDM\_SDA の HDM\_SCL

[Page19] 駱獨LC 3 0.1uH+10pF  
椒橄LVDS DDC pull high,backlight adj箇痼net PWM-ADJ

[Page25] DGPUPRSNT#᠋᠋᠋᠋pull down

[Page30] 3+1\_8VRUN\_PARK\_PWRGDの+1\_0VRUN\_PARK\_PWRGD挡 DGPU\_PWROK

[Page34] C47,C49э 0.1uF

[Page43] Add three X-copper

10 VER

[Page21] Add GPU leakage circuit

[Page12] Reserve TEST\_EN / JTAG\_TMS pull high R for AMD recommend  
Reserve GPIO26\_TCK circuit for AMD recommend  
Reserve JTAG\_TRSTB pull low R for AMD recommend

[Page18] Change D23 P/N to D01-BAS4000-W01  
for HDMI fail

[Page36] Change F9 P/N to D08-0100110-P16  
for USB HDD shut down issue

[Page36] Change C351 P/N to C98-1011650-P01  
for USB HDD shut down issue

[Page31] Stuff R134 for internal speaker POP noise.

[Page45] Add RC delay to follow PARK power sequence.

[Page12] GPIO26\_TCK pull down through 10k R229.

12 VER

[Page5] Add ER47,ER48 22ohm R for OC function.

[Page29] Add SMB\_CLK\_EC/SMB\_DATA\_EC for OC function by EC.

[Page43] Add uP6263 and PR65 for OC function.